



QCA8337N Seven-port Gigabit Ethernet Switch

Datasheet

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Revision History

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3/23/2012	<ul style="list-style-type: none">■ Update pinout and descriptions for pin B1, A3, B2, B3, A5, B10, B12, B14, B19, A33, B29, A47, B46, A56, A61, A63, B63, B69, A80, B70, A81, B71, A82, B72, A83, B73, A84, B74, A85, B75, A86, B76■ Update electrical characteristics	0.2
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Contents

1	General Description	27
1.1	Features	28
1.2	System block diagram	29
2	Pin Descriptions	30
2.1	Pinout diagram	31
2.2	Pin descriptions	32
3	Functional Description	37
3.1	Basic switch function	37
3.1.1	Lookup engine	38
3.1.2	Automatic address learning	38
3.1.3	Automatic address aging	38
3.1.4	Flow control	38
3.1.5	ARL table	39
3.1.6	Mirroring	41
3.2	QoS	41
3.2.1	Scheduling	41
3.2.2	Ingress rate limit	41
3.2.3	Egress rate limit	42
3.2.4	Head-of-line blocking	42
3.3	VLAN	42
3.3.1	Port-based VLAN	42
3.3.2	802.1q VLANs	42
3.3.3	VLAN security	43
3.3.4	Port isolation	43
3.3.5	Leaky VLAN	43
3.3.6	VLAN translation	43
3.3.7	VLAN translation table	44
3.3.8	Egress mode	44
3.3.9	VLAN table	45
3.4	ACL	46
3.4.1	ACL rule	46
3.4.2	Action definition	47

3.4.3	MAC pattern	48
3.4.4	IPv4 pattern	49
3.4.5	IPv6 pattern	51
3.4.6	Window pattern	53
3.4.7	Enhanced MAC pattern	54
3.4.8	Enhanced MAC pattern mask	55
3.5	IGMP/MLD snooping	56
3.5.1	IEEE 802.3 reserved group addresses filtering control	56
3.5.2	802.1x	56
3.5.3	Forwarding unknown	56
3.5.4	MAC limit	56
3.6	Atheros header	57
3.6.1	Transmit	58
3.6.2	Receive	58
3.6.3	Header for read/write register	59
3.7	MIB/statistics counters	60
3.8	LED control	62
3.9	EEPROM programming format	63
3.10	MDC/MDIO access	64
3.11	HNAT	65
3.11.1	Basic NAT table	66
3.11.2	NAPT entry	67
3.11.3	Router MAC address	68
3.11.4	ARP entry	68
3.12	IEEE 802.3az and energy efficient Ethernet	69
3.12.1	IEEE 802.3az LPI mode	70
3.13	Memory map	70
4	Electrical Characteristics	72
4.1	Absolute maximum ratings	72
4.2	Recommended operating conditions	72
4.3	RGMI/GMII characteristics	73
4.4	Power-on strapping	73
4.4.1	Power-on-reset timing	74
4.5	AC timing	74
4.5.1	XTAL/OSC timing	74
4.5.2	MII timing	75
4.5.3	GMII timing	76
4.5.4	RGMI timing	77
4.5.5	SPI timing	77
4.5.6	MDIO timing	78
4.6	Typical power consumption parameters	79

5	Register Descriptions	80
5.1	Register address space (offset range: 0x0000–0x0E98)	80
5.2	Global control registers (offset range: 0x0000–0x00E0)	81
5.2.1	MASK_CTRL	82
5.2.2	PORT0_PAD_CTRL	82
5.2.3	PORT5_PAD_CTRL	84
5.2.4	PORT6_PAD_CTRL	85
5.2.5	PWS_REG	86
5.2.6	GLOBAL_INT0	87
5.2.7	GLOBAL_INT1	88
5.2.8	GLOBAL_INT0_MASK	89
5.2.9	GLOBAL_INT1_MASK	90
5.2.10	MODULE_EN	91
5.2.11	MIB	91
5.2.12	INTERFACE_HIGH_ADDR	92
5.2.13	MDIO master control	93
5.2.14	BIST_CTRL	93
5.2.15	BIST_RECOVER	94
5.2.16	SERVICE_TAG	94
5.2.17	LED_CTRL0	95
5.2.18	LED_CTRL1	95
5.2.19	LED_CTRL2	95
5.2.20	LED_CTRL3	96
5.2.21	GOL_MAC_ADDR0	96
5.2.22	GOL_MAC_ADDR1	97
5.2.23	MAX_FRAME_SIZE	97
5.2.24	PORT0_STATUS	98
5.2.25	PORT1_STATUS	99
5.2.26	PORT2_STATUS	100
5.2.27	PORT3_STATUS	101
5.2.28	PORT4_STATUS	102
5.2.29	PORT5_STATUS	103
5.2.30	PORT6_STATUS	104
5.2.31	HEADER_CTRL	105
5.2.32	PORT0_HEADER_CTRL	105
5.2.33	PORT1_HEADER_CTRL	106
5.2.34	PORT2_HEADER_CTRL	106
5.2.35	PORT3_HEADER_CTRL	107
5.2.36	PORT4_HEADER_CTRL	108
5.2.37	PORT5_HEADER_CTRL	108
5.2.38	PORT6_HEADER_CTRL	109
5.2.39	SGMII_CTRL	109
5.3	EEE control registers (offset range: 0x0100–0x0168)	111

5.3.1	EEE_CTRL	112
5.3.2	EEE_LOC_VALUE_1	113
5.3.3	EEE_REM_VALUE_1	113
5.3.4	EEE_RES_VALUE_1	113
5.3.5	EEE_LOC_VALUE_2	113
5.3.6	EEE_REM_VALUE_2	114
5.3.7	EEE_RES_VALUE_2	114
5.3.8	EEE_LOC_VALUE_3	114
5.3.9	EEE_REM_VALUE_3	115
5.3.10	EEE_RES_VALUE_3	115
5.3.11	EEE_LOC_VALUE_4	115
5.3.12	EEE_REM_VALUE_4	115
5.3.13	EEE_RES_VALUE_4	116
5.3.14	EEE_LOC_VALUE_5	116
5.3.15	EEE_REM_VALUE_5	116
5.3.16	EEE_RES_VALUE_5	117
5.4	Parser control registers (offset range: 0x0200–0x0270)	117
5.4.1	NORMALIZE_CTRL0	117
5.4.2	NORMALIZE_CTRL1	119
5.4.3	NORMALIZE_LEN_CTRL	120
5.4.4	FRAM_ACK_CTRL0	120
5.4.5	FRAM_ACK_CTRL1	121
5.4.6	WIN_RULE_CTRL0	123
5.4.7	WIN_RULE_CTRL1	123
5.4.8	WIN_RULE_CTRL2	124
5.4.9	WIN_RULE_CTRL3	124
5.4.10	WIN_RULE_CTRL4	125
5.4.11	WIN_RULE_CTRL5	125
5.4.12	WIN_RULE_CTRL6	126
5.4.13	WIN_RULE_CTRL7	127
5.4.14	WIN_RULE_CTRL8	127
5.4.15	WIN_RULE_CTRL9	127
5.4.16	WIN_RULE_CTRL10	128
5.4.17	WIN_RULE_CTRL11	128
5.4.18	WIN_RULE_CTRL12	129
5.4.19	WIN_RULE_CTRL13	129
5.4.20	TRUNK_HASH_EN	130
5.5	ACL register (offset range: 0x0400–0x0454)	130
5.5.1	ACL_FUNC0	131
5.5.2	ACL_FUNC1	131
5.5.3	ACL_FUNC2	132
5.5.4	ACL_FUNC3	132
5.5.5	ACL_FUNC4	132

5.5.6	ACL_FUNC5	132
5.5.7	VLAN_TRANS_TEST	133
5.5.8	PORT0_VLAN_CTRL0	133
5.5.9	PORT0_VLAN_CTRL1	133
5.5.10	PORT1_VLAN_CTRL0	134
5.5.11	PORT1_VLAN_CTRL1	135
5.5.12	PORT2_VLAN_CTRL0	136
5.5.13	PORT2_VLAN_CTRL1	136
5.5.14	PORT3_VLAN_CTRL0	137
5.5.15	PORT3_VLAN_CTRL1	138
5.5.16	PORT4_VLAN_CTRL0	139
5.5.17	PORT4_VLAN_CTRL1	139
5.5.18	PORT5_VLAN_CTRL0	140
5.5.19	PORT5_VLAN_CTRL1	141
5.5.20	PORT6_VLAN_CTRL0	142
5.5.21	PORT6_VLAN_CTRL1	142
5.5.22	IPV4_PRI_BASE_ADDR	143
5.5.23	IPV4_PRI_BASE_ADDR_MASK	144
5.6	Lookup register (offset range: 0x0600–0x0718)	144
5.6.1	ATU_DATA0	145
5.6.2	ATU_DATA1	145
5.6.3	ATU_DATA2	146
5.6.4	ATU_FUNC_REG	147
5.6.5	VTU_FUNC_REG0	148
5.6.6	VTU_FUNC_REG1	149
5.6.7	ARL_CTRL	150
5.6.8	GLOBAL_FW_CTRL0	151
5.6.9	GLOBAL_FW_CTRL1	153
5.6.10	GOL_LEARN_LIMIT	153
5.6.11	TOS_PRI_MAP_REG0	154
5.6.12	TOS_PRI_MAP_REG1	154
5.6.13	TOS_PRI_MAP_REG2	155
5.6.14	TOS_PRI_MAP_REG3	155
5.6.15	TOS_PRI_MAP_REG4	156
5.6.16	TOS_PRI_MAP_REG5	156
5.6.17	TOS_PRI_MAP_REG6	157
5.6.18	TOS_PRI_MAP_REG7	157
5.6.19	VLAN_PRI_MAP_REG0	158
5.6.20	LOOP_CHECK_RESULT	158
5.6.21	PORT0_LOOKUP_CTRL	158
5.6.22	PORT0_PRI_CTRL	160
5.6.23	PORT0_LEARN_LIMIT	161
5.6.24	PORT1_LOOKUP_CTRL	162

5.6.25	PORT1_PRI_CTRL	164
5.6.26	PORT1_LEARN_LIMIT	165
5.6.27	PORT2_LOOKUP_CTRL	166
5.6.28	PORT2_PRI_CTRL	167
5.6.29	PORT2_LEARN_LIMIT	168
5.6.30	PORT3_LOOKUP_CTRL	169
5.6.31	PORT3_PRI_CTRL	171
5.6.32	PORT3_LEARN_LIMIT	171
5.6.33	PORT4_LOOKUP_CTRL	172
5.6.34	PORT4_PRI_CTRL	174
5.6.35	PORT4_LEARN_LIMIT	175
5.6.36	PORT5_LOOKUP_CTRL	176
5.6.37	PORT5_PRI_CTRL	178
5.6.38	PORT5_LEARN_LIMIT	179
5.6.39	PORT6_LOOKUP_CTRL	180
5.6.40	PORT6_PRI_CTRL	182
5.6.41	PORT6_LEARN_LIMIT	183
5.6.42	GOL_TRUNK_CTRL0	184
5.6.43	GOL_TRUNK_CTRL1	184
5.6.44	GOL_TRUNK_CTRL2	185
5.6.45	ACL_FWD_SRC_FLTR_CTRL0	185
5.6.46	ACL_FWD_SRC_FLTR_CTRL1	186
5.6.47	ACL_FWD_SRC_FLTR_CTRL2	186
5.7	QM register (offset range: 0x0800–0x0B70)	186
5.7.1	GLOBAL_FLOW_THD	189
5.7.2	QM_CTRL_REG	189
5.7.3	WAN_QUEUE_MAP_REG	190
5.7.4	LAN_QUEUE_MAP_REG	191
5.7.5	PORT0_WRR_CTRL	191
5.7.6	PORT1_WRR_CTRL	192
5.7.7	PORT2_WRR_CTRL	193
5.7.8	PORT3_WRR_CTRL	193
5.7.9	PORT4_WRR_CTRL	194
5.7.10	PORT5_WRR_CTRL	194
5.7.11	PORT6_WRR_CTRL	195
5.7.12	PORT0_EG_RATE_CTRL0	196
5.7.13	PORT0_EG_RATE_CTRL1	196
5.7.14	PORT0_EG_RATE_CTRL2	197
5.7.15	PORT0_EG_RATE_CTRL3	197
5.7.16	PORT0_EG_RATE_CTRL4	198
5.7.17	PORT0_EG_RATE_CTRL5	198
5.7.18	PORT0_EG_RATE_CTRL6	199
5.7.19	PORT0_EG_RATE_CTRL7	203

5.7.20	PORT1_EG_RATE_CTRL0	206
5.7.21	PORT1_EG_RATE_CTRL1	207
5.7.22	PORT1_EG_RATE_CTRL2	207
5.7.23	PORT1_EG_RATE_CTRL3	208
5.7.24	PORT1_EG_RATE_CTRL4	208
5.7.25	PORT1_EG_RATE_CTRL5	209
5.7.26	PORT2_EG_RATE_CTRL0	210
5.7.27	PORT2_EG_RATE_CTRL1	211
5.7.28	PORT2_EG_RATE_CTRL2	211
5.7.29	PORT2_EG_RATE_CTRL3	212
5.7.30	PORT2_EG_RATE_CTRL4	212
5.7.31	PORT2_EG_RATE_CTRL5	213
5.7.32	PORT3_EG_RATE_CTRL0	214
5.7.33	PORT3_EG_RATE_CTRL1	214
5.7.34	PORT3_EG_RATE_CTRL2	215
5.7.35	PORT3_EG_RATE_CTRL3	215
5.7.36	PORT3_EG_RATE_CTRL4	216
5.7.37	PORT3_EG_RATE_CTRL5	217
5.7.38	PORT4_EG_RATE_CTRL0	217
5.7.39	PORT4_EG_RATE_CTRL1	218
5.7.40	PORT4_EG_RATE_CTRL2	218
5.7.41	PORT4_EG_RATE_CTRL3	219
5.7.42	PORT4_EG_RATE_CTRL4	219
5.7.43	PORT4_EG_RATE_CTRL5	220
5.7.44	PORT5_EG_RATE_CTRL0	221
5.7.45	PORT5_EG_RATE_CTRL1	222
5.7.46	PORT5_EG_RATE_CTRL2	222
5.7.47	PORT5_EG_RATE_CTRL3	223
5.7.48	PORT5_EG_RATE_CTRL4	223
5.7.49	PORT5_EG_RATE_CTRL5	224
5.7.50	PORT5_EG_RATE_CTRL6	224
5.7.51	PORT5_EG_RATE_CTRL7	225
5.7.52	PORT6_EG_RATE_CTRL0	226
5.7.53	PORT6_EG_RATE_CTRL1	227
5.7.54	PORT6_EG_RATE_CTRL2	227
5.7.55	PORT6_EG_RATE_CTRL3	228
5.7.56	PORT6_EG_RATE_CTRL4	228
5.7.57	PORT6_EG_RATE_CTRL5	229
5.7.58	PORT6_EG_RATE_CTRL6	229
5.7.59	PORT6_EG_RATE_CTRL7	230
5.7.60	PORT0_HOL_CTRL0	231
5.7.61	PORT0_HOL_CTRL1	232
5.7.62	PORT1_HOL_CTRL0	232

5.7.63	PORT1_HOL_CTRL1	233
5.7.64	PORT2_HOL_CTRL0	234
5.7.65	PORT2_HOL_CTRL1	235
5.7.66	PORT3_HOL_CTRL0	235
5.7.67	PORT3_HOL_CTRL1	236
5.7.68	PORT4_HOL_CTRL0	237
5.7.69	PORT4_HOL_CTRL1	237
5.7.70	PORT5_HOL_CTRL0	238
5.7.71	PORT5_HOL_CTRL1	239
5.7.72	PORT6_HOL_CTRL0	239
5.7.73	PORT6_HOL_CTRL1	240
5.7.74	PORT0_FLOW_THD	241
5.7.75	PORT1_FLOW_THD	241
5.7.76	PORT2_FLOW_THD	242
5.7.77	PORT3_FLOW_THD	242
5.7.78	PORT4_FLOW_THD	243
5.7.79	PORT5_FLOW_THD	243
5.7.80	PORT6_FLOW_THD	244
5.7.81	ACL_POLICY_MODE	244
5.7.82	ACL_COUNTER_MODE	245
5.7.83	ACL_CNT_RESET	247
5.7.84	ACL_RATE_CTRL0_0	248
5.7.85	ACL_RATE_CTRL1_0	248
5.7.86	ACL_RATE_CTRL0_1	249
5.7.87	ACL_RATE_CTRL1_1	249
5.7.88	ACL_RATE_CTRL0_2	250
5.7.89	ACL_RATE_CTRL1_2	250
5.7.90	ACL_RATE_CTRL0_3	251
5.7.91	ACL_RATE_CTRL1_3	252
5.7.92	ACL_RATE_CTRL0_4	252
5.7.93	ACL_RATE_CTRL1_4	253
5.7.94	ACL_RATE_CTRL0_5	253
5.7.95	ACL_RATE_CTRL1_5	254
5.7.96	ACL_RATE_CTRL0_6	254
5.7.97	ACL_RATE_CTRL1_6	255
5.7.98	ACL_RATE_CTRL0_7	255
5.7.99	ACL_RATE_CTRL1_7	256
5.7.100	ACL_RATE_CTRL0_8	256
5.7.101	ACL_RATE_CTRL1_8	257
5.7.102	ACL_RATE_CTRL0_9	257
5.7.103	ACL_RATE_CTRL1_9	258
5.7.104	ACL_RATE_CTRL0_10	258
5.7.105	ACL_RATE_CTRL1_10	259

5.7.106	ACL_RATE_CTRL0_11	259
5.7.107	ACL_RATE_CTRL1_11	260
5.7.108	ACL_RATE_CTRL0_12	260
5.7.109	ACL_RATE_CTRL1_12	261
5.7.110	ACL_RATE_CTRL0_13	261
5.7.111	ACL_RATE_CTRL1_13	262
5.7.112	ACL_RATE_CTRL0_14	262
5.7.113	ACL_RATE_CTRL1_14	263
5.7.114	ACL_RATE_CTRL0_15	263
5.7.115	ACL_RATE_CTRL1_15	264
5.7.116	ACL_RATE_CTRL0_16	264
5.7.117	ACL_RATE_CTRL1_16	265
5.7.118	ACL_RATE_CTRL0_17	265
5.7.119	ACL_RATE_CTRL1_17	266
5.7.120	ACL_RATE_CTRL0_18	266
5.7.121	ACL_RATE_CTRL0_18	267
5.7.122	ACL_RATE_CTRL0_19	267
5.7.123	ACL_RATE_CTRL1_19	268
5.7.124	ACL_RATE_CTRL0_20	268
5.7.125	ACL_RATE_CTRL1_20	269
5.7.126	ACL_RATE_CTRL0_21	269
5.7.127	ACL_RATE_CTRL1_21	270
5.7.128	ACL_RATE_CTRL0_22	270
5.7.129	ACL_RATE_CTRL1_22	271
5.7.130	ACL_RATE_CTRL0_23	271
5.7.131	ACL_RATE_CTRL1_23	272
5.7.132	ACL_RATE_CTRL0_24	272
5.7.133	ACL_RATE_CTRL1_24	273
5.7.134	ACL_RATE_CTRL0_25	273
5.7.135	ACL_RATE_CTRL1_25	274
5.7.136	ACL_RATE_CTRL0_26	275
5.7.137	ACL_RATE_CTRL1_26	275
5.7.138	ACL_RATE_CTRL0_27	276
5.7.139	ACL_RATE_CTRL1_27	276
5.7.140	ACL_RATE_CTRL0_28	277
5.7.141	ACL_RATE_CTRL1_28	277
5.7.142	ACL_RATE_CTRL0_29	278
5.7.143	ACL_RATE_CTRL1_29	278
5.7.144	ACL_RATE_CTRL0_30	279
5.7.145	ACL_RATE_CTRL1_30	279
5.7.146	ACL_RATE_CTRL0_31	280
5.7.147	ACL_RATE_CTRL1_31	280
5.7.148	PORT0_ING_RATE_CTRL0	281

5.7.149	PORT0_ING_RATE_CTRL1	281
5.7.150	PORT0_ING_RATE_CTRL2	282
5.7.151	PORT1_ING_RATE_CTRL0	283
5.7.152	PORT1_ING_RATE_CTRL1	284
5.7.153	PORT1_ING_RATE_CTRL2	284
5.7.154	PORT2_ING_RATE_CTRL0	285
5.7.155	PORT2_ING_RATE_CTRL1	286
5.7.156	PORT2_ING_RATE_CTRL2	287
5.7.157	PORT3_ING_RATE_CTRL0	288
5.7.158	PORT3_ING_RATE_CTRL1	289
5.7.159	PORT3_ING_RATE_CTRL2	289
5.7.160	PORT4_ING_RATE_CTRL0	290
5.7.161	PORT4_ING_RATE_CTRL1	291
5.7.162	PORT4_ING_RATE_CTRL2	292
5.7.163	PORT5_ING_RATE_CTRL0	293
5.7.164	PORT5_ING_RATE_CTRL1	294
5.7.165	PORT5_ING_RATE_CTRL2	294
5.7.166	PORT6_ING_RATE_CTRL0	295
5.7.167	PORT6_ING_RATE_CTRL1	296
5.7.168	PORT6_ING_RATE_CTRL2	297
5.7.169	CPU_GROUP_CTRL	298
5.8	PKT edit register (offset range: 0x0C00–0x0C80)	299
5.8.1	PKT_EDIT_CTRL	299
5.8.2	PORT0_QUEUE_REMAP_REG0	300
5.8.3	PORT0_QUEUE_REMAP_REG1	301
5.8.4	PORT1_QUEUE_REMAP_REG0	301
5.8.5	PORT2_QUEUE_REMAP_REG0	301
5.8.6	PORT3_QUEUE_REMAP_REG0	302
5.8.7	PORT4_QUEUE_REMAP_REG0	303
5.8.8	PORT5_QUEUE_REMAP_REG0	303
5.8.9	PORT5_QUEUE_REMAP_REG1	304
5.8.10	PORT6_QUEUE_REMAP_REG0	304
5.8.11	PORT6_QUEUE_REMAP_REG1	305
5.8.12	Router default VID register 0	305
5.8.13	Router default VID register 1	306
5.8.14	Router default VID register 2	306
5.8.15	Router default VID register 3	306
5.8.16	Router egress VLAN mode	306
5.9	Layer 3 register (offset range: 0x0E00–0x0E98)	307
5.9.1	HROUTER_CONTROL	308
5.9.2	HROUTER_PBASED_CONTROL0	309
5.9.3	HROUTER_PBASED_CONTROL1	309
5.9.4	HROUTER_PBASED_CONTROL2	309

5.9.5	WCMP_HASH_TABLE0	310
5.9.6	WCMP_HASH_TABLE1	310
5.9.7	WCMP_HASH_TABLE2	311
5.9.8	WCMP_HASH_TABLE3	311
5.9.9	WCMP_NHOP_TABLE0	311
5.9.10	WCMP_NHOP_TABLE1	312
5.9.11	WCMP_NHOP_TABLE2	312
5.9.12	WCMP_NHOP_TABLE3	312
5.9.13	ARP_ENTRY_LOCK_CONTROL	313
5.9.14	ARP_USED_ACCOUNT	313
5.9.15	HNAT_CONTROL	313
5.9.16	NAPT_ENTRY_LOCK_CONTROL0	315
5.9.17	NAPT_ENTRY_LOCK_CONTROL1	315
5.9.18	NAPT_USED_ACCOUNT	315
5.9.19	ENTRY_EDIT_DATA0	316
5.9.20	ENTRY_EDIT_DATA1	316
5.9.21	ENTRY_EDIT_DATA2	316
5.9.22	ENTRY_EDIT_DATA3	316
5.9.23	ENTRY_EDIT_DATA4	317
5.9.24	ENTRY_EDIT_DATA5	317
5.9.25	ENTRY_EDIT_DATA6	317
5.9.26	ENTRY_EDIT_CONTROL	317
5.10	PHY control registers	319
5.10.1	Control register	321
5.10.2	Status Register	322
5.10.3	PHY identifier	324
5.10.4	PHY Identifier 2	324
5.10.5	Auto-negotiation advertisement register	325
5.10.6	Link partner ability register	327
5.10.7	Auto-negotiation expansion register	329
5.10.8	Next page transmit register	329
5.10.9	Link partner next page register	330
5.10.10	1000BASE-T control register	331
5.10.11	1000BASE-T status register	333
5.10.12	MMD access control register	334
5.10.13	MMD access address data register	334
5.10.14	Extended status register	334
5.10.15	Function control register	335
5.10.16	PHY-specific status register	336
5.10.17	Interrupt enable register	338
5.10.18	Interrupt status register	339
5.10.19	Smart speed register	341
5.10.20	Receive error counter register	342

5.10.21	Virtual cable tester control register	342
5.10.22	Virtual cable tester status register	343
5.10.23	Debug port	344
5.10.24	Debug port 2 (R/W port)	344
5.11	Debug register	344
5.11.1	Analog test control	344
5.11.2	System mode control	346
5.11.3	System control mode	347
5.11.4	HIB control and auto-negotiation test register	348
5.11.5	RGMII mode selection	350
5.11.6	Green feature configure register	351
5.12	MMD3 — PCS register	352
5.12.1	PCS control1	352
5.12.2	PCS status1	352
5.12.3	EEE capability register	353
5.12.4	EEE wake error counter	353
5.13	MMD7 — auto-negotiation register	354
5.13.1	AN package	354
5.13.2	AN status	355
5.13.3	AN XNP transmit	356
5.13.4	AN XNP transmit1	356
5.13.5	AN XNP transmit 2	356
5.13.6	AN LP XNP ability	356
5.13.7	AN LP XNP ability1	357
5.13.8	AN LP XNP ability2	357
5.13.9	EEE advertisement	357
5.13.10	EEE LP advertisement	358
5.13.11	EEE ability auto-negotiation result	359
6	Package Dimensions	360
7	Ordering Information	362
8	Top-Side Marking	363

Figures

Figure 1-1 QCA8337N system block diagram	29
Figure 2-1 QCA8337N pinout diagram (148-pin DR-QFN)	31
Figure 3-1 Read/write register command frame format	59
Figure 3-2 EEPROM programming format	64
Figure 3-3 MDC/MDIO access format	65
Figure 3-4 Operating power modes—802.3az LIP mode	70
Figure 4-1 Power-on-reset timing diagram	74
Figure 4-2 XTAL/OSC timing diagram	75
Figure 4-3 MII input timing diagram	76
Figure 4-4 1000BASE-T GMII timing diagram	76
Figure 4-5 RGMII timing diagram	77
Figure 4-6 EEPROM interface timing diagram	78
Figure 4-7 MDIO timing diagram	78
Figure 6-1 148-pin DR-QFN package drawing	360
Figure 8-1 Top-side marking	363
Figure 8-2 Top-side marking	363

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Tables

Table 2-1 Signal to pin descriptions	32
Table 2-2 Interface summary	36
Table 3-1 ARL table	39
Table 3-2 Reserved ATU entry	40
Table 3-3 Ingress VLAN mode	43
Table 3-4 VLAN security	43
Table 3-5 VLAN translation table	44
Table 3-6 VLAN egress mode — tagging	44
Table 3-7 VLAN egress mode	45
Table 3-8 VLAN table format	45
Table 3-9 ACL patterns	46
Table 3-10 Action definition	47
Table 3-11 MAC pattern	48
Table 3-12 MAC pattern mask	49
Table 3-13 IPv4 pattern	49
Table 3-14 IPv4 mask	50
Table 3-15 IPv6 pattern 1	51
Table 3-16 IPv6 pattern 2	51
Table 3-17 IPv6 pattern 3	51
Table 3-18 IPv6 Mask 1	52
Table 3-19 IPv6 mask 2	52
Table 3-20 IPv6 mask 3	53
Table 3-21 Window pattern	53
Table 3-22 Window pattern mask	54
Table 3-23 Enhanced MAC pattern	54
Table 3-24 Enhanced MAC pattern mask	55
Table 3-25 Type definition for Atheros header	57
Table 3-26 Atheros header transmit format	58
Table 3-27 Atheros header receive	58
Table 3-28 Command format for read/write register using Atheros header	59
Table 3-29 MIB counters	60
Table 3-30 LED control	62
Table 3-31 LED rule default value	63
Table 3-32 Basic NAT	66
Table 3-33 NAPT entry	67
Table 3-34 Router MAC address	68
Table 3-35 ARP entry	69
Table 3-36 Memory map	70
Table 4-1 Absolute maximum ratings	72

Table 4-2 Recommended operating conditions	72
Table 4-3 RGMII/GMII DC characteristics	73
Table 4-4 Power-on-strapping	73
Table 4-5 XTAL/OSC timing	75
Table 4-6 MII timing	76
Table 4-7 1000BASE-T GMII timing	77
Table 4-8 Reduced GMII timing	77
Table 4-9 EEPROM interface timing	78
Table 4-10 MDIO timing	78
Table 4-11 Total system power (1000BASE-T)	79
Table 5-1 Register reset types	80
Table 5-2 Register address space summary	81
Table 5-3 Global control registers summary	81
Table 5-4 MASK_CTRL bit description	82
Table 5-5 PORT0_PAD_CTRL bit description	83
Table 5-6 PORT5_PAD_CTRL bit description	84
Table 5-7 PORT6_PAD_CTRL bit description	85
Table 5-8 PWS_REG bit description	86
Table 5-9 GLOBAL_INT0 bit description	87
Table 5-10 GLOBAL_INT1 bit description	89
Table 5-11 GLOBAL_INT0_MASK bit description	89
Table 5-12 GLOBAL_INT1_MASK bit description	90
Table 5-13 MODULE_EN bit description	91
Table 5-14 MIB bit description	92
Table 5-15 INTERFACE_HIGH_ADDR bit description	92
Table 5-16 MDIO master control bit description	93
Table 5-17 BIST_CTRL bit description	94
Table 5-18 BIST_RECOVER bit description	94
Table 5-19 SERVICE_TAG bit description	95
Table 5-20 LED_CTRL0 bit description	95
Table 5-21 LED_CTRL1 bit description	95
Table 5-22 LED_CTRL2 bit description	96
Table 5-23 LED_CTRL3 bit description	96
Table 5-24 GLOL_MAC_ADDR0 bit description	97
Table 5-25 GLOL_MAC_ADDR1 bit description	97
Table 5-26 MAX_FRAME_SIZE bit description	97
Table 5-27 PORT0_STATUS bit description	98
Table 5-28 PORT1_STATUS bit description	99
Table 5-29 PORT2_STATUS bit description	100
Table 5-30 PORT 3_STATUS bit description	101
Table 5-31 PORT4_STATUS bit description	102
Table 5-32 PORT 5_STATUS bit description	103
Table 5-33 PORT 6_STATUS bit description	104

Table 5-34	HEADER_CTRL bit description	105
Table 5-35	PORT_HEADER_CTRL bit description	105
Table 5-36	PORT1_HEADER_CTRL bit description	106
Table 5-37	PORT 2_HEADER_CTRL bit description	107
Table 5-38	PORT3_HEADER_CTRL bit description	107
Table 5-39	PORT4_HEADER_CTRL bit description	108
Table 5-40	PORT5_HEADER_CTRL bit description	108
Table 5-41	PORT6_HEADER_CTRL bit description	109
Table 5-42	SGMII_CTRL bit description	110
Table 5-43	EEE control register summary	112
Table 5-44	EEE_CTRL bit description	112
Table 5-45	EEE_LOC_VALUE1 bit description	113
Table 5-46	EEE_REM_VALUE_1 bit description	113
Table 5-47	EEE_RES_VALUE_1 bit description	113
Table 5-48	EEE_LOC_VALUE_2 bit description	114
Table 5-49	EEE_REM_VALUE_2 bit description	114
Table 5-50	EEE_RES_VALUE_2 bit description	114
Table 5-51	EEE_LOC_VALUE_3 bit description	114
Table 5-52	EEE_REM_VALUE_3 bit description	115
Table 5-53	EEE_RES_VALUE_3 bit description	115
Table 5-54	EEE_LOC_VALUE_4 bit description	115
Table 5-55	EEE_REM_VALUE_4 bit description	116
Table 5-56	EEE_RES_VALUE_4 bit description	116
Table 5-57	EEE_LOC_VALUE_5 bit description	116
Table 5-58	EEE_REM_VALUE_5 bit description	116
Table 5-59	EEE_RES_VALUE_5 bit description	117
Table 5-60	Parser register summary	117
Table 5-61	NORMALIZE_CTRL0 bit description	117
Table 5-62	NORMALIZE_CTRL1 bit description	119
Table 5-63	NORMALIZE_LEN_CTRL bit description	120
Table 5-64	FRAM_ACK_CTRL0 bit description	120
Table 5-65	FRAM_ACK_CTRL1 bit description	122
Table 5-66	WIN_RULE_CTRL0 bit description	123
Table 5-67	WIN_RULE_CTRL1 bit description	123
Table 5-68	WIN_RULE_CTRL2 bit description	124
Table 5-69	WIN_RULE_CTRL3 bit description	124
Table 5-70	WIN_RULE_CTRL4 bit description	125
Table 5-71	WIN_RULE_CTRL5 bit description	126
Table 5-72	WIN_RULE_CTRL6 bit description	126
Table 5-73	WIN_RULE_CTRL7 bit description	127
Table 5-74	WIN_RULE_CTRL8 bit description	127
Table 5-75	WIN_RULE_CTRL9 bit description	128
Table 5-76	WIN_RULE_CTRL10 bit description	128

Table 5-77 WIN_RULE_CTRL11 bit description	129
Table 5-78 WIN_RULE_CTRL12 bit description	129
Table 5-79 WIN_RULE_CTRL13 bit description	130
Table 5-80 TRUNK_HASH_EN bit description	130
Table 5-81 ACL register summary	130
Table 5-82 ACL_FUNC0 bit description	131
Table 5-83 ACL_FUNC1 bit description	131
Table 5-84 ACL_FUNC2 bit description	132
Table 5-85 ACL_FUNC3 bit description	132
Table 5-86 ACL_FUNC4 bit description	132
Table 5-87 ACL_FUNC5 bit description	132
Table 5-88 VLAN_TRANS_TEST bit description	133
Table 5-89 PORT0_VLAN_CTRL0 bit description	133
Table 5-90 PORT0_VLAN_CTRL1 bit description	134
Table 5-91 PORT1_VLAN_CTRL0 bit description	135
Table 5-92 PORT1_VLAN_CTRL1 bit description	135
Table 5-93 PORT2_VLAN_CTRL0 bit description	136
Table 5-94 PORT2_VLAN_CTRL1 bit description	137
Table 5-95 PORT3_VLAN_CTRL0 bit description	138
Table 5-96 PORT3_VLAN_CTRL1 bit description	138
Table 5-97 PORT4_VLAN_CTRL0 bit description	139
Table 5-98 PORT4_VLAN_CTRL1 bit description	140
Table 5-99 PORT5_VLAN_CTRL0 bit description	141
Table 5-100 PORT5_VLAN_CTRL1 bit description	141
Table 5-101 PORT6_VLAN_CTRL0 bit description	142
Table 5-102 PORT6_VLAN_CTRL1 bit description	143
Table 5-103 IPV4_PRI_BASE_ADDR bit description	143
Table 5-104 IPV4_PRI_BASE_ADDR_MASK bit description	144
Table 5-105 Lookup register summary	144
Table 5-106 ATU_DATA0 bit description	145
Table 5-107 ATU_DATA1 bit description	146
Table 5-108 TU_DATA2 bit description	146
Table 5-109 ATU_FUNC_REG bit description	147
Table 5-110 VTU_FUNC_REG0 bit description	149
Table 5-111 VTU_FUNC_REG1 bit description	149
Table 5-112 ARL_CTRL bit description	150
Table 5-113 GLOBAL_FW_CTRL0 bit description	151
Table 5-114 GLOBAL_FW_CTRL1 bit description	153
Table 5-115 GOL_LEARN_LIMIT bit description	154
Table 5-116 TOS_PRI_MAP_REG0 bit description	154
Table 5-117 TOS_PRI_MAP_REG1 bit description	155
Table 5-118 TOS_PRI_MAP_REG2 bit description	155
Table 5-119 TOS_PRI_MAP_REG3 bit description	155

Table 5-120	TOS_PRI_MAP_REG4 bit description	156
Table 5-121	TOS_PRI_MAP_REG5 bit description	156
Table 5-122	TOS_PRI_MAP_REG6 bit description	157
Table 5-123	TOS_PRI_MAP_REG7 bit description	157
Table 5-124	VLAN_PRI_MAP_REG0 bit description	158
Table 5-125	LOOP_CHECK_RESULT bit description	158
Table 5-126	PORT0_LOOKUP_CTRL bit description	159
Table 5-127	PORT0_PRI_CTRL bit description	161
Table 5-128	PORT0_LEARN_LIMIT bit description	161
Table 5-129	PORT1_LOOKUP_CTRL bit description	162
Table 5-130	PORT1_PRI_CTRL bit description	164
Table 5-131	PORT1_LEARN_LIMIT bit description	165
Table 5-132	PORT2_LOOKUP_CTRL bit description	166
Table 5-133	PORT2_PRI_CTRL bit description	167
Table 5-134	PORT2_LEARN_LIMIT bit description	168
Table 5-135	PORT3_LOOKUP_CTRL bit description	169
Table 5-136	PORT3_PRI_CTRL bit description	171
Table 5-137	PORT3_LEARN_LIMIT bit description	172
Table 5-138	PORT4_LOOKUP_CTRL bit description	172
Table 5-139	PORT4_PRI_CTRL bit description	175
Table 5-140	PORT4_LEARN_LIMIT bit description	175
Table 5-141	PORT5_LOOKUP_CTRL bit description	176
Table 5-142	PORT5_PRI_CTRL bit description	179
Table 5-143	PORT5_LEARN_LIMIT bit description	179
Table 5-144	PORT6_LOOKUP_CTRL bit description	180
Table 5-145	PORT6_PRI_CTRL bit description	182
Table 5-146	PORT6_LEARN_LIMIT bit description	183
Table 5-147	GOL_TRUNK_CTRL0 bit description	184
Table 5-148	GOL_TRUNK_CTRL1 bit description	184
Table 5-149	GOL_TRUNK_CTRL2 bit description	185
Table 5-150	ACL_FWD_SRC_FLTR_CTRL0 bit description	186
Table 5-151	ACL_FWD_SRC_FLTR_CTRL1 bit description	186
Table 5-152	ACL_FWD_SRC_FLTR_CTRL2 bit description	186
Table 5-153	QM register summary	186
Table 5-154	GLOBAL_FLOW_THD bit description	189
Table 5-155	QM_CTRL_REG bit description	189
Table 5-156	WAN_QUEUE_MAP_REG bit description	190
Table 5-157	LAN_QUEUE_MAP_REG bit description	191
Table 5-158	PORT0_WRR_CTRL bit description	192
Table 5-159	PORT1_WRR_CTRL bit description	192
Table 5-160	PORT2_WRR_CTRL bit description	193
Table 5-161	PORT3_WRR_CTR bit description	193
Table 5-162	PORT4_WRR_CTRL bit description	194

Table 5-163	PORT5_WRR_CTRL bit description	195
Table 5-164	PORT6_WRR_CTRL bit description	195
Table 5-165	PORT0_EG_RATE_CTRL0 bit description	196
Table 5-166	PORT0_EG_RATE_CTRL1 bit description	196
Table 5-167	PORT0_EG_RATE_CTRL2 bit description	197
Table 5-168	PORT0_EG_RATE_CTRL3 bit description	197
Table 5-169	PORT0_EG_RATE_CTRL4 bit description	198
Table 5-170	PORT0_EG_RATE_CTRL5 bit description	198
Table 5-171	PORT0_EG_RATE_CTRL6 bit description	199
Table 5-172	PORT0_EG_RATE_CTRL7 bit description	204
Table 5-173	PORT1_EG_RATE_CTRL0 bit description	207
Table 5-174	PORT1_EG_RATE_CTRL1 bit description	207
Table 5-175	PORT1_EG_RATE_CTRL2 bit description	208
Table 5-176	PORT1_EG_RATE_CTRL3 bit description	208
Table 5-177	PORT1_EG_RATE_CTRL4 bit description	209
Table 5-178	PORT1_EG_RATE_CTRL5 bit description	209
Table 5-179	PORT2_EG_RATE_CTRL0 bit description	210
Table 5-180	PORT2_EG_RATE_CTRL1 bit description	211
Table 5-181	PORT2_EG_RATE_CTRL2 bit description	211
Table 5-182	PORT2_EG_RATE_CTRL3 bit description	212
Table 5-183	PORT2_EG_RATE_CTRL4 bit description	212
Table 5-184	PORT2_EG_RATE_CTRL5 bit description	213
Table 5-185	PORT3_EG_RATE_CTRL0 bit description	214
Table 5-186	PORT3_EG_RATE_CTRL1 bit description	215
Table 5-187	PORT3_EG_RATE_CTRL2 bit description	215
Table 5-188	PORT3_EG_RATE_CTRL3 bit description	216
Table 5-189	PORT3_EG_RATE_CTRL4 bit description	216
Table 5-190	PORT3_EG_RATE_CTRL5 bit description	217
Table 5-191	PORT4_EG_RATE_CTRL0 bit description	218
Table 5-192	PORT4_EG_RATE_CTRL1 bit description	218
Table 5-193	PORT4_EG_RATE_CTRL2 bit description	219
Table 5-194	PORT4_EG_RATE_CTRL3 bit description	219
Table 5-195	PORT4_EG_RATE_CTRL4 bit description	220
Table 5-196	PORT4_EG_RATE_CTRL5 bit description	220
Table 5-197	PORT5_EG_RATE_CTRL0 bit description	221
Table 5-198	PORT5_EG_RATE_CTRL1 bit description	222
Table 5-199	PORT5_EG_RATE_CTRL2 bit description	222
Table 5-200	PORT5_EG_RATE_CTRL3 bit description	223
Table 5-201	PORT5_EG_RATE_CTRL4 bit description	223
Table 5-202	PORT5_EG_RATE_CTRL5 bit description	224
Table 5-203	PORT5_EG_RATE_CTRL6 bit description	224
Table 5-204	PORT5_EG_RATE_CTRL7 bit description	225
Table 5-205	PORT6_EG_RATE_CTRL0 bit description	226

Table 5-206	PORT6_EG_RATE_CTRL1 bit description	227
Table 5-207	PORT6_EG_RATE_CTRL2 bit description	227
Table 5-208	PORT6_EG_RATE_CTRL3 bit description	228
Table 5-209	PORT6_EG_RATE_CTRL4 bit description	228
Table 5-210	PORT6_EG_RATE_CTRL5 bit description	229
Table 5-211	PORT6_EG_RATE_CTRL6 bit description	229
Table 5-212	PORT6_EG_RATE_CTRL7 bit description	230
Table 5-213	PORT0_HOL_CTRL0 bit description	231
Table 5-214	PORT0_HOL_CTRL1 bit description	232
Table 5-215	PORT1_HOL_CTRL0 bit description	233
Table 5-216	PORT1_HOL_CTRL1 bit description	233
Table 5-217	PORT2_HOL_CTRL0 bit description	234
Table 5-218	PORT2_HOL_CTRL1 bit description	235
Table 5-219	PORT3_HOL_CTRL0 bit description	235
Table 5-220	PORT3_HOL_CTRL1 bit description	236
Table 5-221	PORT4_HOL_CTRL0 bit description	237
Table 5-222	PORT4_HOL_CTRL1 bit description	237
Table 5-223	PORT5_HOL_CTRL0 bit description	238
Table 5-224	PORT5_HOL_CTRL1 bit description	239
Table 5-225	PORT6_HOL_CTRL0 bit description	240
Table 5-226	PORT6_HOL_CTRL1 bit description	240
Table 5-227	PORT0_FLOW_THD bit description	241
Table 5-228	PORT1_FLOW_THD bit description	241
Table 5-229	PORT2_FLOW_THD bit description	242
Table 5-230	PORT3_FLOW_THD bit description	242
Table 5-231	PORT4_FLOW_THD bit description	243
Table 5-232	PORT5_FLOW_THD bit description	243
Table 5-233	PORT6_FLOW_THD bit description	244
Table 5-234	ACL_POLICY_MODE bit description	244
Table 5-235	ACL_COUNTER_MODE bit description	246
Table 5-236	ACL_CNT_RESET bit description	247
Table 5-237	ACL_RATE_CTRL0_0 bit description	248
Table 5-238	ACL_RATE_CTRL1_0 bit description	248
Table 5-239	ACL_RATE_CTRL0_1 bit description	249
Table 5-240	ACL_RATE_CTRL1_1 bit description	250
Table 5-241	ACL_RATE_CTRL0_2 bit description	250
Table 5-242	ACL_RATE_CTRL1_2 bit description	251
Table 5-243	ACL_RATE_CTRL0_3 bit description	251
Table 5-244	ACL_RATE_CTRL1_3 bit description	252
Table 5-245	ACL_RATE_CTRL0_4 bit description	252
Table 5-246	ACL_RATE_CTRL1_4 bit description	253
Table 5-247	ACL_RATE_CTRL0_5 bit description	253
Table 5-248	ACL_RATE_CTRL1_5 bit description	254

Table 5-249	ACL_RATE_CTRL0_6 bit description	254
Table 5-250	ACL_RATE_CTRL1_6 bit description	255
Table 5-251	ACL_RATE_CTRL0_7 bit description	255
Table 5-252	ACL_RATE_CTRL1_7 bit description	256
Table 5-253	ACL_RATE_CTRL0_8 bit description	256
Table 5-254	ACL_RATE_CTRL1_8 bit description	257
Table 5-255	ACL_RATE_CTRL0_9 bit description	257
Table 5-256	ACL_RATE_CTRL1_9 bit description	258
Table 5-257	ACL_RATE_CTRL0_10 bit description	258
Table 5-258	ACL_RATE_CTRL1_10 bit description	259
Table 5-259	ACL_RATE_CTRL0_11 bit description	259
Table 5-260	ACL_RATE_CTRL1_11 bit description	260
Table 5-261	ACL_RATE_CTRL0_12 bit description	260
Table 5-262	ACL_RATE_CTRL1_12 bit description	261
Table 5-263	ACL_RATE_CTRL0_13 bit description	261
Table 5-264	ACL_RATE_CTRL1_13 bit description	262
Table 5-265	ACL_RATE_CTRL0_14 bit description	262
Table 5-266	ACL_RATE_CTRL1_14 bit description	263
Table 5-267	ACL_RATE_CTRL0_15 bit description	263
Table 5-268	ACL_RATE_CTRL1_15 bit description	264
Table 5-269	ACL_RATE_CTRL0_16 bit description	264
Table 5-270	ACL_RATE_CTRL1_16 bit description	265
Table 5-271	ACL_RATE_CTRL1_17 bit description	265
Table 5-272	ACL_RATE_CTRL1_17 bit description	266
Table 5-273	ACL_RATE_CTRL0_18 bit description	266
Table 5-274	ACL_RATE_CTRL1_18 bit description	267
Table 5-275	ACL_RATE_CTRL0_19 bit description	267
Table 5-276	ACL_RATE_CTRL1_19 bit description	268
Table 5-277	ACL_RATE_CTRL0_20 bit description	268
Table 5-278	ACL_RATE_CTRL1_20 bit description	269
Table 5-279	ACL_RATE_CTRL0_21 bit description	269
Table 5-280	ACL_RATE_CTRL1_21 bit description	270
Table 5-281	ACL_RATE_CTRL0_22 bit description	270
Table 5-282	ACL_RATE_CTRL1_22 bit description	271
Table 5-283	ACL_RATE_CTRL0_23 bit description	272
Table 5-284	ACL_RATE_CTRL1_23 bit description	272
Table 5-285	ACL_RATE_CTRL0_24 bit description	273
Table 5-286	ACL_RATE_CTRL1_24 bit description	273
Table 5-287	ACL_RATE_CTRL0_25 bit description	274
Table 5-288	ACL_RATE_CTRL1_25 bit description	274
Table 5-289	ACL_RATE_CTRL0_26 bit description	275
Table 5-290	ACL_RATE_CTRL1_26 bit description	275
Table 5-291	ACL_RATE_CTRL0_27 bit description	276

Table 5-292	ACL_RATE_CTRL1_27 bit description	276
Table 5-293	ACL_RATE_CTRL0_28 bit description	277
Table 5-294	ACL_RATE_CTRL1_28 bit description	277
Table 5-295	ACL_RATE_CTRL0_29 bit description	278
Table 5-296	ACL_RATE_CTRL1_29 bit description	278
Table 5-297	ACL_RATE_CTRL0_30 bit description	279
Table 5-298	ACL_RATE_CTRL1_30 bit description	279
Table 5-299	ACL_RATE_CTRL0_31 bit description	280
Table 5-300	ACL_RATE_CTRL1_31 bit description	280
Table 5-301	PORT0_ING_RATE_CTRL0 bit description	281
Table 5-302	PORT0_ING_RATE_CTRL1 bit description	281
Table 5-303	PORT0_ING_RATE_CTRL2 bit description	282
Table 5-304	PORT1_ING_RATE_CTRL0 bit description	283
Table 5-305	PORT1_ING_RATE_CTRL1 bit description	284
Table 5-306	PORT1_ING_RATE_CTRL2 bit description	285
Table 5-307	PORT2_ING_RATE_CTRL0 bit description	286
Table 5-308	PORT2_ING_RATE_CTRL1 bit description	286
Table 5-309	PORT2_ING_RATE_CTRL2 bit description	287
Table 5-310	PORT3_ING_RATE_CTRL0 bit description	288
Table 5-311	PORT3_ING_RATE_CTRL1 bit description	289
Table 5-312	PORT3_ING_RATE_CTRL2 bit description	290
Table 5-313	PORT4_ING_RATE_CTRL0 bit description	291
Table 5-314	PORT4_ING_RATE_CTRL1 bit description	291
Table 5-315	PORT4_ING_RATE_CTRL2 bit description	292
Table 5-316	PORT5_ING_RATE_CTRL0 bit description	293
Table 5-317	PORT5_ING_RATE_CTRL1 bit description	294
Table 5-318	PORT5_ING_RATE_CTRL2 bit description	295
Table 5-319	PORT6_ING_RATE_CTRL0 bit description	296
Table 5-320	PORT6_ING_RATE_CTRL1 bit description	296
Table 5-321	PORT6_ING_RATE_CTRL2 bit description	297
Table 5-322	CPU_GROUP_CTRL bit description	298
Table 5-323	Packet editor register summary	299
Table 5-324	PKT_EDIT_CTRL bit description	299
Table 5-325	PORT0_QUEUE_REMAP_REG0 bit description	300
Table 5-326	PORT0_QUEUE_REMAP_REG0 bit description	301
Table 5-327	PORT1_QUEUE_REMAP_REG0 bit description	301
Table 5-328	PORT2_QUEUE_REMAP_REG0 bit description	302
Table 5-329	PORT3_QUEUE_REMAP_REG0 bit description	302
Table 5-330	PORT4_QUEUE_REMAP_REG0 bit description	303
Table 5-331	PORT5_QUEUE_REMAP_REG0 bit description	303
Table 5-332	PORT5_QUEUE_REMAP_REG1 bit description	304
Table 5-333	PORT6_QUEUE_REMAP_REG0 bit description	304
Table 5-334	PORT6_QUEUE_REMAP_REG1 bit description	305

Table 5-335 Router default VID register 0 bit description	305
Table 5-336 Router default VID register 1 bit description	306
Table 5-337 Router default VID register 2 bit description	306
Table 5-338 Router default VID register 3 bit description	306
Table 5-339 Router egress VLAN mode bit description	307
Table 5-340 Layer 3 register summary	307
Table 5-341 HROUTER_CONTROL bit description	308
Table 5-342 HROUTER_PBASED_CONTROL0 bit description	309
Table 5-343 HROUTER_PBASED_CONTROL1 bit description	309
Table 5-344 HROUTER_PBASED_CONTROL2 bit description	310
Table 5-345 WCMP_HASH_TABLE0 bit description	310
Table 5-346 WCMP_HASH_TABLE1 bit description	311
Table 5-347 WCMP_HASH_TABLE2 bit description	311
Table 5-348 WCMP_HASH_TABLE3 bit description	311
Table 5-349 WCMP_NHOP_TABLE0 bit description	311
Table 5-350 WCMP_NHOP_TABLE1 bit description	312
Table 5-351 WCMP_NHOP_TABLE2 bit description	312
Table 5-352 WCMP_NHOP_TABLE3 bit description	312
Table 5-353 ARP_ENTRY_LOCK_CONTROL bit description	313
Table 5-354 ARP_USED_ACCOUNT bit description	313
Table 5-355 HNAT_CONTROL bit description	314
Table 5-356 NAPT_ENTRY_LOCK_CONTROL0 bit description	315
Table 5-357 NAPT_ENTRY_LOCK_CONTROL1 bit description	315
Table 5-358 NAPT_USED_ACCOUNT bit description	316
Table 5-359 ENTRY_EDIT_DATA0 bit description	316
Table 5-360 ENTRY_EDIT_DATA1 bit description	316
Table 5-361 ENTRY_EDIT_DATA2 bit description	316
Table 5-362 ENTRY_EDIT_DATA3 bit description	317
Table 5-363 ENTRY_EDIT_DATA4 bit description	317
Table 5-364 ENTRY_EDIT_DATA5 bit description	317
Table 5-365 ENTRY_EDIT_DATA6 bit description	317
Table 5-366 ENTRY_EDIT_CONTROL bit description	318
Table 5-367 PHY control register summary	319
Table 5-368 PHY control register summary — MMD3	320
Table 5-369 PHY control register summary — MMD7	320
Table 5-370 Control register bit description	321
Table 5-371 Status registers bit description	322
Table 5-372 PHY Identifier bit description	324
Table 5-373 PHY Identifier 2 bit description	324
Table 5-374 Auto-negotiation advertisement register bit description	325
Table 5-375 Link partner ability bit description	327
Table 5-376 Auto-negotiation expansion bit description	329
Table 5-377 Next page transmit register bit description	329

Table 5-378	link partner next page bit description	330
Table 5-379	1000BASE-T control bit description	331
Table 5-380	1000BASE-T status bit description	333
Table 5-381	MMD access control bit description	334
Table 5-382	MMD access address data register bit description	334
Table 5-383	Extended status register bit description	335
Table 5-384	Function control register bit description	335
Table 5-385	PHY-specific status register bit description	336
Table 5-386	Interrupt enable register bit description	338
Table 5-387	Interrupt status register bit description	340
Table 5-388	Smart speed register bit description	341
Table 5-389	Status register bit description	342
Table 5-390	Virtual cable tester control register bit description	343
Table 5-391	Virtual cable tester status register bit description	343
Table 5-392	Debug port (address offset 0x1d, or 0d29) bit description	344
Table 5-393	Debug port 2 (R/W port) bit description	344
Table 5-394	Analog test control bit description	345
Table 5-395	System mode control bit description	346
Table 5-396	System control mode bit description	347
Table 5-397	HIB control and auto-negotiation test register bit description	348
Table 5-398	RGMII mode selection bit description	350
Table 5-399	Green feature configure register bit description	351
Table 5-400	PCS control1 bit description	352
Table 5-401	PCS status1 bit description	352
Table 5-402	EEE capability register bit description	353
Table 5-403	EEE wake error counter bit description	354
Table 5-404	AN control 1 bit description	354
Table 5-405	AN package bit description	355
Table 5-406	AN status bit description	355
Table 5-407	AN XNP transmit bit description	356
Table 5-408	AN XNP transmit1 bit description	356
Table 5-409	AN XNP transmit2 bit description	356
Table 5-410	AN LP XNP ability bit description	357
Table 5-411	AN LP XNP ability1 bit description	357
Table 5-412	AN LP XNP ability2 bit description	357
Table 5-413	EEE advertisement bit description	358
Table 5-414	EEE LP advertisement bit description	358
Table 5-415	EEE ability auto-negotiation result bit description	359
Table 6-1	Package dimensions (in mm)	361
Table 7-1	Ordering information	362
Table 8-1	Top-side marking	363

1 General Description

The QCA8337N is a highly integrated seven-port Gigabit Ethernet switch with non-blocking switch fabric, a high-performance lookup unit with 2048 MAC addresses, and a four-traffic class Quality of Service (QoS) engine. The QCA8337N switch has the flexibility to support various networking applications. The QCA8337N is designed for cost-sensitive switch applications in high end gateway and xPON.

The QCA8337N integrates all the functions of a high-speed switch system, including packet buffer, PHY transceivers, media access controllers, address management, and a non-blocking switch fabric into a single 55 nm CMOS device. It complies with 10BASE-T_e, and 1000BASE-T specifications, including MAC control, pause frame, and auto-negotiation subsections, providing compatibility with all industry standard Ethernet, Fast Ethernet and Gigabit Ethernet.

The QCA8337N device contains five full-duplex 10BASE-T_e/100BASE-T_x/1000BASE-T transceivers and 10BASE-T_e /100BASE-T_x can run at half-duplex, each of which performs all of the physical layer interface functions for 10BASE-T_e Ethernet on category 5 unshielded twisted-pair (UTP) cable and Fast/Gigabit Ethernet on category 5 UTP cable.

The remaining two ports feature a standard GMII/RGMII/MII/SerDes interface to allow connection to host CPU in PON/xDSL/cable/Wi-Fi/fiber routers. The media access controllers on the QCA8337N also support jumbo frames which are typically used for high-performance connections to servers because they offer a smaller percentage of overhead on the link for more efficiency.

SPI or EEPROM interfaces provide easy programming of the on-chip 802.1p QoS and/or DiffServ/TOS. This allows switch traffic to be given different classes of priority or service — for example, voice traffic for IP phone applications, video traffic for multimedia applications, or data traffic for email applications.

Up to 4K virtual LANs (VLANs) can be set up via the SPI port for separation of different users or groups on the network. ACL feature can reduce CPU effort for VLAN/QoS/DSCP/forward mapping and remapping based on layer 1 to layer 4 information. PPPoE header add/removal can increase video quality and offload CPU loading. Hardware IGMP V1/V2/V3 is an innovation for IPTV service. Green ETHOS® power saving technologies can increase energy efficiency for no link or idle state.

The QCA8337N supports the following configuration:

- 5 ports of 10/100/1000BASE-T + 1 port of GMII/RGMII/MII+1 port of SerDes
- 5 ports of 10/100/1000BASE-T + 2 ports of RGMII/MII
- 4 ports of 10/100/1000BASE-T + 1 ports of RGMII/MII + 1 port single RGMII PHY

The QCA8337N supports the following modes of network address translation (NAT):

- Basic NAT: This involves IP address translation only, no port mapping.
- Network address and port translation (NAPT): This involves the translation of both IP addresses and port numbers. For the NAPT mode, the QCA8337N can support full-cone NAT, restricted cone NAT, port-restricted cone NAT and symmetric NAT.

The QCA8337N chip supports hardware network address translation (HNAT) to offload the CPU and achieve full wire speed when doing NAT.

1.1 Features

- Support 802.3az power management
- ACL mask rule from layer 1 to layer 4. Port number, destination address, source address, Ethernet type, VLAN, IP protocol, IPv4/IPv6 source/destination address, TCP/UDP source/destination port.
- 96 ACL mask rule for pass/drop, VLAN/QoS/DSCP mapping/translation
- User-defined ACL, up to 48 bytes depth in layer 4/3/2
- QoS mechanisms include Weighted Round Robin (WRR), strict, hybrid up queue
- Port-based VLAN and 4K 802.1q VLAN group
- IVL and SVL
- IGMP snooping V1, V2 and V3. IPv6 MLD V1/V2 forwarded to CPU
- Support light hardware IGMP snooping V1/V2/V3, MLD V1/V2 and smart leave
- Hardware looping detection
- QinQ function for SVLAN & CVLAN translation
- IP packet/PPPoE bypass to reduce CPU loading on video packet
- 16 PPPoE session support/PPP session header removal/addition
- Scalable ingress/egress bandwidth control
- 40 MIBs counter/port and port status
- 1M bit packet buffer
- Support 9K jumbo frame
- Port mirror, 802.1X security, Rapid Spanning Tree
- Rule-based bandwidth control
- Programmable Wake-on-LAN (WoL)
- Half power mode for cable length less than 30 m (for home installations)
- Support internal/external loopback
- Support reduced AFE circuit
- 2K MAC table, edit, search, add & delete.
- MAC limit by port/chip/VLAN

- Trunking function
- Support trunking and auto-failover
- Power saving on cable no link, short cable & 10BASE-T idle
- Support VLAN translation and mapping with 64 translation entries
- Support 100/1000 FX on SerDes port
- Support thermal meter with resolution 3°C–5°C and thermal interrupt register
- Support 1K NAPT entries and 128 hardware-based host routing (ARP) entries
- Support hardware-based IP source guard, ARP inspection, routing/layer 3 switching
- Support programmable CPU port on RGMII 0 and RGMII 1 interface
- The QCA8337N chip includes hardware network address translation (HNAT) function; the QCA8337 chip (without the N designation) does not include the hardware NAT function.
- 148-pin DR-QFN, 55 nm

1.2 System block diagram

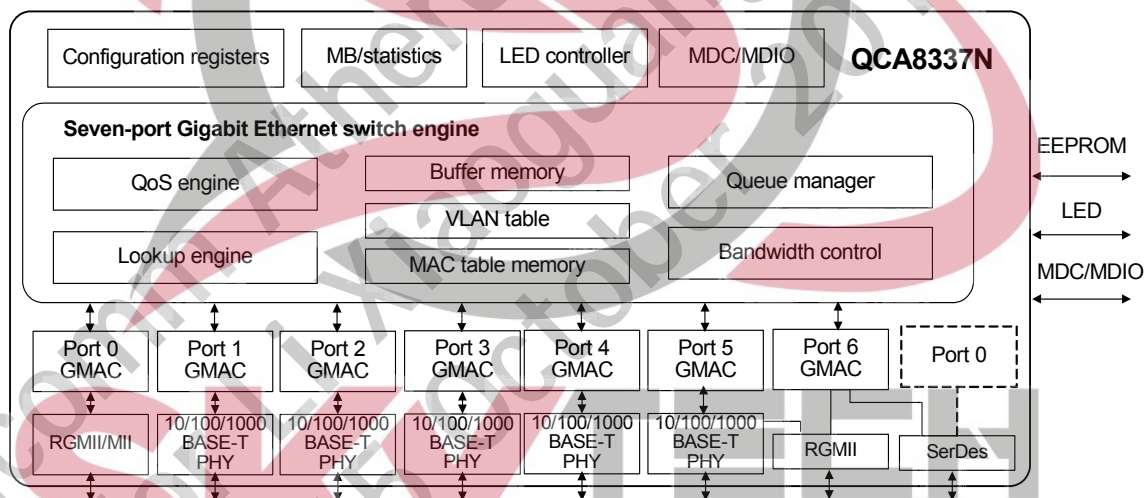


Figure 1-1 QCA8337N system block diagram

2 Pin Descriptions

This section contains a listing of the signal descriptions (see [Table 2-1](#) and [Figure 2-1](#)).

The following nomenclature is used for signal names:

- _L At the end of the signal name, indicating active low signals
- N At the end of the signal name, indicating the negative side of a differential signal
- NC No connection should be made to this pin
- P At the end of the signal name, indicating the positive side of a differential signal

The following nomenclature is used for signal types:

- D Open drain for digital pads
- I Digital input signal
- I/O Digital bidirectional signal
- IA Analog input signal
- IH Digital input with hysteresis
- IL Input signals with weak internal pull-down, to prevent signals from floating when left open
- O Digital output signal
- OA Analog output signal
- P A power or ground signal
- PD Internal pull-down for digital input
- PU Internal pull-up for digital input

2.1 Pinout diagram

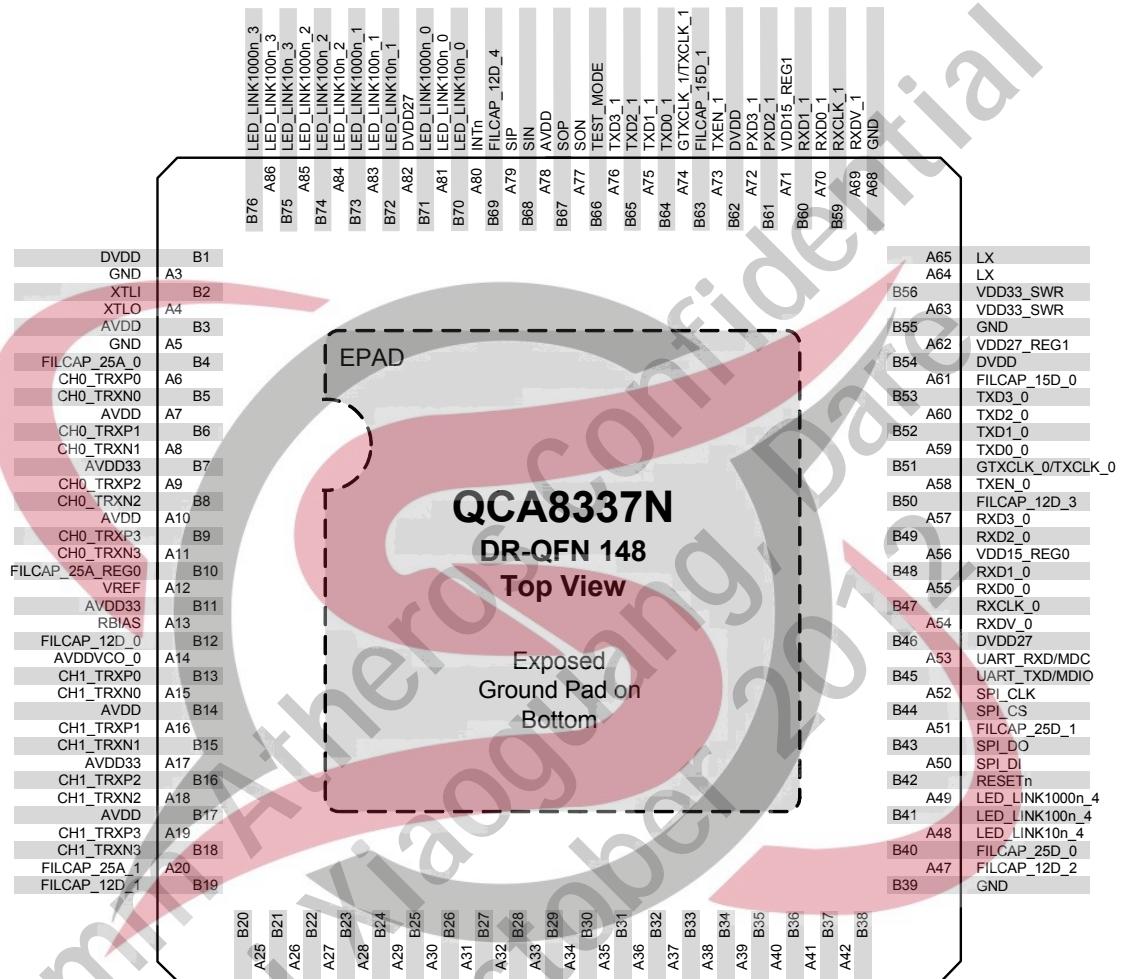


Figure 2-1 QCA8337N pinout diagram (148-pin DR-QFN)

2.2 Pin descriptions

Table 2-1 Signal to pin descriptions

Signal name	Pin	Type	Description
Media-dependent interface			
CH0_TRXN0	B5	IA,OA	Media-dependent interface, MDI[3:0]: Transmitter output positive/negative Connect directly to transformer without any pull-down terminators, such as resistors or capacitors, required.
CH0_TRXP0	A6	IA,OA	
CH0_TRXN1	A8	IA,OA	
CH0_TRXP1	B6	IA,OA	
CH0_TRXN2	B8	IA,OA	
CH0_TRXP2	A9	IA,OA	
CH0_TRXN3	A11	IA,OA	
CH0_TRXP3	B9	IA,OA	
CH1_TRXN0	A15	IA,OA	
CH1_TRXP0	B13	IA,OA	
CH1_TRXN1	B15	IA,OA	
CH1_TRXP1	A16	IA,OA	
CH1_TRXN2	A18	IA,OA	
CH1_TRXP2	B16	IA,OA	
CH1_TRXN3	B18	IA,OA	
CH1_TRXP3	A19	IA,OA	
CH2_TRXN0	A25	IA,OA	Media-dependent interface, MDI[3:0]: Transmitter output positive/negative Connect directly to transformer without any pull-down terminators, such as resistors or capacitors, required.
CH2_TRXP0	B20	IA,OA	
CH2_TRXN1	B22	IA,OA	
CH2_TRXP1	A26	IA,OA	
CH2_TRXN2	A28	IA,OA	
CH2_TRXP2	B23	IA,OA	
CH2_TRXN3	B25	IA,OA	
CH2_TRXP3	A29	IA,OA	
CH3_TRXN0	A31	IA,OA	
CH3_TRXP0	B26	IA,OA	
CH3_TRXN1	B28	IA,OA	
CH3_TRXP1	A32	IA,OA	
CH3_TRXN2	A35	IA,OA	
CH3_TRXP2	B30	IA,OA	
CH3_TRXN3	B32	IA,OA	
CH3_TRXP3	A36	IA,OA	

Table 2-1 Signal to pin descriptions (cont.)

Signal name	Pin	Type	Description
CH4_TRXN0	A38	IA,OA	Media-dependent interface, MDI[3:0]: Transmitter output positive/negative Connect directly to transformer without any pull-down terminators, such as resistors or capacitors, required.
CH4_TRXP0	B33	IA,OA	
CH4_TRXN1	B35	IA,OA	
CH4_TRXP1	A39	IA,OA	
CH4_TRXN2	A41	IA,OA	
CH4_TRXP2	B36	IA,OA	
CH4_TRXN3	B38	IA,OA	
CH4_TRXP3	A42	IA,OA	
RGMI/MII interface 0			
GTXCLK_0/TXCLK_0	B51	I/O	RGMI/MII transmit clock, 125 MHz, 25 MHz or configurable. This is the reference clock for RGMI/MII or MII mode.
RXCLK_0	B47	I/O	RGMI/MII receive clock. This is the reference clock for RGMI/MII or MII mode.
RXDV_0	A54	I/O,PU	RGMI/MII received data; valid. This is output signal for MAC controller.
RXD0_0	A55	I/O, PD	RGMI/MII receive data or configuration; RXD[3:0]_0 are used as data output when operating in RGMI/MII or MII mode. The reference clock for these output signals is RXCLK_0 (pin B47).
RXD1_0	B48	I/O, PD	
RXD2_0	B49	I/O, PU	
RXD3_0	A57	I/O, PD	
TXEN_0	A58	I	RGMI/MII transmit enable. This is input signal for the MAC controller.
TXD0_0	A59	I	RGMI/MII transmit data. These are input signals for MAC controller. TXD[3:0]_0 are used as data input when operating in RGMI/MII or MII mode. The reference clock for these input signals is GTXCLK_0(pin B51).
TXD1_0	B52	I	
TXD2_0	A60	I	
TXD3_0	B53	I	
RGMI/MII interface 1			
GTXCLK_1/TXCLK_1	A74	I/O	RGMI/MII transmit clock, 125 MHz, 25 MHz or configurable. This is the reference clock for RGMI/MII or MII mode.
RXCLK_1	B59	I/O	RGMI/MII receive clock. This is the reference clock for RGMI/MII or MII mode.
RXDV_1	A69	I/O, PD	RGMI/MII received data; valid. This is output signal for MAC controller.
RXD0_1	A70	I/O, PD	RGMI/MII receive data or configuration. RXD[3:0]_1 are used as data output when operating in RGMI/MII or MII mode. The reference clock for these output signals is RXCLK_1(pin B59).
RXD1_1	B60	I/O, PD	
RXD2_1	B61	I/O, PD	
RXD3_1	A72	I/O, PD	
TXEN_1	A73	I	RGMI/MII transmit enable. This is input signal for the MAC controller.

Table 2-1 Signal to pin descriptions (cont.)

Signal name	Pin	Type	Description
TXD0_1	B64	I	RGMII/MII transmit data. These are input signals for MAC controller. TXD[3:0]_1 are used as data input when operating in RGMII or MII mode. The reference clock for these input signals is GTXCLK_1(pin A74).
TXD1_1	A75	I	
TXD2_1	B65	I	
TXD3_1	A76	I	
LED			
LED_LINK10n_0	B70	O,D	LED_LINK10n_[4:0]
LED_LINK10n_1	B72	O,D	Parallel LED output for 10BASE-T _e link/speed/activity, active low. The LED inactive state can be open-drain or driving high output, depending on the power-on strapping setup. The LED behaviour can be configurable, see the LED control registers (0x0050–0x005C). The register offset 0x0058 is for 10BASE-T _e .
LED_LINK10n_2	A84	O,D	
LED_LINK10n_3	B75	O,D	
LED_LINK10n_4	A48	O,D	
LED_LINK100n_0	A81	O,D	LED_LINK100n_[4:0]
LED_LINK100n_1	A83	O,D	Parallel LED output for 100BASE-T _x link/speed/activity, active low. The LED inactive state can be open-drain or driving high output, depending on the power-on strapping. The LED behaviour can be configured, see the LED control registers (0x0050–0x005C). The register offset 0x0054 is for 100BASE-T _x .
LED_LINK100n_2	B74	O,D	
LED_LINK100n_3	A86	O,D	
LED_LINK100n_4	B41	O,D	
LED_LINK1000n_0	B71	O,D	LED_LINK1000n_[4:0]
LED_LINK1000n_1	B73	O,D	Parallel LED output for 1000BASE-T link/speed/activity, active low. The LED inactive state can be open-drain or driving high output, depending on the power-on strapping setup. The LED behaviour can be configured, see the LED control registers (0x0050–0x005C). The register offset 0x0050 is for 1000BASE-T.
LED_LINK1000n_2	A85	O,D	
LED_LINK1000n_3	B76	O,D	
LED_LINK1000n_4	A49	O,D	
UART/MDIO and SPI EEPROM			
SPI_CLK	A52	I/O, PD	SPI clock
SPI_CS	B44	I/O, PD	SPI chip selection
SPI_DI	A50	I, PD	SPI data input
SPI_DO	B43	I/O, PU	SPI data output
UART_RXD/MDC	A53	I, PD	Management data clock reference
UART_TXD/MDIO	B45	I/O	Management data
SerDes interface			
SOP	B67	OA	SerDes differential output pair
SON	A77	OA	
SIP	A79	IA	SerDes differential input pair
SIN	B68	IA	
Miscellaneous			
RBIAS	A13	OA	Connect 2.37 kΩ resistor to GND. The resistor value is adjustable, depending on PCB.
RESETn	B42	IH	Chip reset, active low. The active low duration must be greater than 10 ms.

Table 2-1 Signal to pin descriptions (cont.)

Signal name	Pin	Type	Description
TEST_MODE	B66	I	Test mode: 0 = Normal operation 1 = Test mode
XTLI	B2	IA	Crystal oscillator input, connect a 27 pF capacitor to GND. An external 25 MHz clock with swing from 0-1 V can be injected to this pin. When an external clock source is used, the 27 pF capacitor should be removed from this pin and the 27 pF capacitor at XTLO should be maintained.
XTLO	A4	OA	Crystal oscillator output, connect a 27 pF capacitor to GND
INTn	A80	O, PU	Interrupt, active low. See the global interrupt registers (0x0020–0x0024).
VREF	A12	OA	Reference voltage, put a 1 nF cap to GND
Power			
DVDD	B1 B54 B62	P	Digital 1.2 V power input
AVDD	B3 A7 A10 B14 B17 B21 B24 B27 A33 B31 B34 B37 A78	P	Analog 1.2 V power input
GND	A3 A5 B39 B55 A68 EPAD	P	Ground
AVDD33	B7 B11 A17 A27 A30 A37 A40	P	Analog 3.3 V power input.

Table 2-1 Signal to pin descriptions (cont.)

Signal name	Pin	Type	Description
VDD33_SWR	B56 A63	P	The 3.3 V power for internal switching regulator
DVDD27	B46 A82	P	2.7 V power input for I/O PAD excluding RGMII interface.
LX	A64 A65	OA	Internal switching regulator output; connect to an inductor 4.7 μ H, 1 A to generate 1.2 V power.
VDD27_REG1	A62	P	2.7 V power output for DVDD27; connect to an external capacitor 1 μ F for power supply stabilization
VDD15_REG0	A56	P	RGMII interface 0 power source. It can be connected to external 2.5 V power or only connect an external capacitor 0.1 μ F and using internal LDO for 1.8 V or 1.5 V interface power.
VDD15_REG1	A71	P	RGMII interface 1 power source. It can be connected to external 2.5 V power or only connect an external capacitor 0.1 μ F and using internal LDO for 1.8 V or 1.5 V interface power.
AVDDVCO_0	A14	P	Analog 1.2 LDO output filter pin for VCO
AVDDVCO_1	B29	P	
FILCAP_25A_REG0	B10	P	Connect to an external capacitor 0.1 μ F for power supply stabilization.
FILCAP_25A_0	B4	P	
FILCAP_25A_1	A20	P	
FILCAP_25A_2	A34	P	
FILCAP_25D_0	B40	P	Connect to an external capacitor 0.1 μ F for power supply stabilization.
FILCAP_25D_1	A51	P	
FILCAP_15D_0	A61	P	Connect to an external capacitor 0.1 μ F for power supply stabilization.
FILCAP_15D_1	B63	P	
FILCAP_12D_0	B12	P	Connect to an external capacitor 0.1 μ F for power supply stabilization.
FILCAP_12D_1	B19	P	
FILCAP_12D_2	A47	P	
FILCAP_12D_3	B50	P	
FILCAP_12D_4	B69	P	

Table 2-2 Interface summary

Mode	MAC 0	MAC 6	MAC 5 or PHY 4
Mode 1	RGMII/MII	RGMII/MII	–
Mode 2	SGMII	RGMII/MII	–
Mode 3	GMII/RGMII/MII	SGMII	–
Mode 4	RGMII/MII	SGMII	MAC 5: RGMII/MII
Mode 5	RGMII/MII	SGMII	PHY 4: RGMII/MII

3 Functional Description

The QCA8337N supports operating modes that can be configured using a low-cost serial EEPROM and/or the MDC/MDIO interface. The QCA8337N also supports a CPU header mode that appends two bytes to each frame.

The CPU can deheader frame with header to configure the switch register, the address lookup table, and VLAN and receive auto-cast MIB frames. The QCA8337N supports single PHY interface as a WAN port. The first port (port0) supports a MAC interface and can be configured in GMII/RGMII-PHY mode to connect to an external management CPU or an integrated CPU in a routing or xDSL engine.

The QCA8337N contains a 2K entry address lookup table that employs three entries per bucket to avoid hash collision and maintain non-blocking forwarding performance. The table also provides read/write accesses from the serial and CPU interfaces; each entry can be configured as a static entry. The QCA8337N supports 4K VLAN entries configurable as port-based VLANs or 802.1q tag-based VLANs.

To provide non-blocking switching performance in all traffic environments, the QCA8337N supports several types of QoS function with four-level priority queues based on port, IEEE 802.1p, IPv4 DSCP, IPv6 TC, 802.1q VID, or MAC address. Back pressure and IEEE 802.3x pause frame-based flow control schemes are included to support zero packet loss under temporary traffic congestion.

Meeting current service provider requirements, the QCA8337N switch uses the latest Qualcomm Atheros QoS switch architecture that supports ingress policing and egress rate limiting. The QCA8337N device supports IPv4 IGMP snooping and IPv6 MLD snooping to significantly improve the performance of streaming media and other bandwidth-intensive IP multicast applications.

A broadcast storm control mechanism prevents the packets from flooding into other parts of the network. The QCA8337N device has an intelligent switch engine to prevent head-of-line blocking problems on per-CoS basis for each port.

3.1 Basic switch function

The QCA8337N automatically learns the port number of an attached end station by looking at the source MAC address of all incoming packets at wire speed. If the source address is not found in the address table, the QCA8337N device adds it to the table. Once the MAC address/port number mapping is learned, all packets directed to that end station's MAC address are forwarded to the learned port number only.

When the QCA8337N device receives incoming packets from one of its ports, it searches in its address table for the destination MAC address, then forwards the packet to the appropriate port within the VLAN group. If the destination MAC address is not found (i.e. a new, unlearned MAC address), the QCA8337N handles the packet as a broadcast packet and transmits it to all ports within the VLAN group, except to the port where it comes in.

3.1.1 Lookup engine

The QCA8337N lookup engine or ARL (Address Resolution Logic) retrieves the DA and SA from each frame received from each port. The ARL performs all address searching, learning, and aging functions at wire speed. The ARL engine uses a hashing algorithm for fast storage and retrieval of address entries. To avoid hash collision, the QCA8337N uses a three-entry bin per hash location that stores up to three MAC addresses at each hash location. The address database is stored in the embedded SRAM and has a size of 2048 entries.

3.1.2 Automatic address learning

Up to 2048 MAC address/port number mappings can be stored in the address table. A three-way hash algorithm allows a maximum of three different addresses with the same hash key to be stored simultaneously. The QCA8337N searches for the SA of an incoming packet in the address table.

If the SA is not found, the address is hashed and stored in the first empty bin found at the hashed location. If all address bins are full, each entry's age time is examined to select the least recently used bin.

If the SA is found, the aging value of the corresponding entry is reset to 0x7. If the DA is dropped due to error or pause frame, the QCA8337N does not perform learning process for this frame.

3.1.3 Automatic address aging

Address aging supports network topology changes such as an end station disconnecting from the network or an address moving from one port to another. An address is removed (aged-out) from the address database after a specified amount of time since the last time it appears in an incoming frame source address. The QCA8337N has a default aging time of 5 minutes, and can be set in 7-second increments to a maximum of 10,000 minutes.

3.1.4 Flow control

The QCA8337N device supports IEEE 802.3x full-duplex flow control, force-mode full-duplex flow control, and half-duplex backpressure.

If the link partner supports auto-negotiation, the 802.3x full-duplex flow control is auto-negotiated between the remote node and the QCA8337N. If the full-duplex flow control is enabled, when the buffer number used for specific port exceed the per port buffer threshold or total buffer used exceeds global based buffer threshold, the QCA8337N sends out an IEEE 802.3x compliant pause frame to stop the remote device from sending more frames.

Half-duplex flow control regulates the remote station to avoid dropping packets in network congestion. Backpressure is supported for half-duplex operations. When the free buffer space is almost empty, the QCA8337N device transmits a jam pattern on the port and forces a collision. If the half-duplex flow control mode is not set, the incoming packet is dropped if there is no buffer space available.

3.1.5 ARL table

The address database is stored in the embedded SRAM and has a size of 2048 entries with a default aging time of about 300 seconds or 5 minutes.

The ARL table supports:

- Search one address in the table
- Use Get Next to read out whole table
- Load and purge an entry in the ARL table
- Flush entries:
 - All entries
 - All non-static entries
 - One port's all entries
 - One port's all non-static entries

All registers and counters can be accessed (read and written) through the UART/MDIO interface and CPU port frames. Interrupts may be asserted upon access completion.

Table 3-1 ARL table

Bits	Name	Description
83:72	VID	The VID group indicates to which the MAC address belongs.
71	RESERVED	
70	COPY_TO_CPU	1 = Packets received with this address should be copied to the CPU port
69	REDIRECT_TO_CPU	1 = Packets received with this address should be redirected to the CPU port. If no CPU is connected to the switch, this frame should be discarded.
68	LEAKY_EN	1 = Use leaky VLAN enable for this MAC address. This bit can be used for unicast and multicast frame controlled by ARL_UNI_LEAKY_EN AND ARL_MULTI_LEAKY_EN.
67:64	STATUS	4'h0: Empty entry 4'h1–4'h7: Dynamic and valid entry 4'h8–4'hE: Reserved 4'F: Entry is static and is not aged out or changed by hardware.
63	RESERVED	
62	SA_DROP_EN	Drop packet enable when source address is in this entry. If this bit is set to 1, the packet with SA of this entry are dropped.

Table 3-1 ARL table (cont.)

Bits	Name	Description
61	MIRROR_EN	0 = Packets should only be sent to destination port 1 = Packets should be sent to mirror port and destination port.
60	PRI_EN	Priority override enable 1 = PRIORITY (ATU[58:56]) can override any other priority determined by the frame's data.
59	SVL_ENTRY	0 = IVL learned 1 = SVL learned
58:56	PRIORITY	The priority bits may be used as the frame's priority when PRI_OVER_EN (bit[60]) is set to 1.
55	CROSS_PORT_STATE_EN	0 = Cross port state disable 1 = Cross port state enable
54:48	DES_PORT	Indicate which ports are associated with this MAC address when they are set to 1. Bit[48] is assigned to port0, bit[49] to port1, bit[50] to port3, and so on. If all bits are set to 0 and the entry is static, the packet should be dropped. For multicast address and unicast for link aggregation, more than one bit is set to 1.
47:0	ADDRESS	48-bit MAC address

Table 3-2 Reserved ATU entry

Bit	Name	Description
64	STATUS	0 = Invalid 1 = Static and valid
63	COPY_TO_CPU	1 = Packets received with the address should be copied to the CPU port
62	REDIRECT_TO_CPU	1 = Packets received with this address should be redirected to the CPU port. If no CPU is connected to the switch, the packet is dropped.
61	LEAKY_EN	1 = Use leaky VLAN enable for this MAC address. This bit can be used for unicast and multicast frames, controlled by ARL_UNI_LEAKY_EN and ARL_MULTI_LEAKY_EN.
60	MIRROR_EN	0 = Packets should be sent only to the destination port 1 = Packets should be sent to the mirror port and the destination port
59	PRI_OVER_EN	Priority override enable 1 = PRIORITY (ATU[58:56]) can override any other priority determined by the frame's data
58:56	PRI	This priority bit may be used as a frame's priority when PRI_OVER_EN is set to 1.
55	CROSS_PORT_STATE_EN	1 = Cross port state enabled
54:48	DES_PORT	These bits indicate which ports are associated with this MAC address when they are set to 1. Bit[48] is assigned to port0, bit[49] to port1, bit[50] to port2, etc.
47:0	ADDRESS	48-bit MAC address

3.1.6 Mirroring

Mirroring monitors traffic for information gathering or troubleshooting higher layer protocol operations. User can specify a desired mirrored port (sniffer port) to receive a copy of all traffic passing through a designated mirrored port.

The QCA8337N supports mirror frames that:

- Come from an ingress-specified port (ingress mirroring)
- Destined for egress-specified port (egress mirroring)
- Mirror all ingress and egress traffic to a designated port
- Mirror frames when configuring the ARL table with mirror enabled
- ACL mirror

3.2 QoS

3.2.1 Scheduling

For the QCA8337N, ports MAC0, MAC5, and MAC6 support six queues while ports MAC1, MAC2, MAC3 and MAC4 support four queues. This egress queue schedule mechanism can be configured to one of the following modes:

- Strict priority (SP)
- Weighted fair queuing
- Only highest queue uses strict priority; others use weighted fair queuing scheme
- The highest two queues use strict priority; other queues use weighted fair queuing scheme

The scheduling mode is configurable per port-based.

The QCA8337N recognizes the QoS information of ingress frames and maps to different egress priority levels. The QCA8337N determines the priority of the frames based on DA, TOS/TC, VLAN, and port. Each has an enable bit that can be applied. When more than one type of priority is selected, the order in which the frame priority should be applied can be determined. Priority enable bits and select order bits are set on a per port basis at the port's base address.

3.2.2 Ingress rate limit

In triple-play applications, the switch may need to limit the rate for all frames but continue to maintain QoS policy. The QCA8337N supports ingress and egress rate limiting requirements on a per-port basis by configuring the port rate limit register.

Ingress rate limit can include or exclude the consideration of management frames and registered multicast frames. The QCA8337N can limit all frames and support rate limits from 32 Kbps to 1 Gbps, at 32 Kbps granularity.

3.2.3 Egress rate limit

The QCA8337N can also support per port or per queue based egress rate limiting. The QCA8337N can support egress rate limits from 32 Kbps to 1 Gbps, at 32 Kbps granularity.

3.2.4 Head-of-line blocking

The QCA8337N supports ingress port buffer and egress port/queue buffer control to handle head-of-line blocking. The maximum queue depth for per port or per queue is configurable. Each port has dedicated buffer resource and this can avoid HOL. The dedicated buffer resource can be configured per queue based and/or per port-based for egress port. When the egress queue depth is over the **configured number**, the ingress frame destination to this queue is dropped if the flow control of source port is disabled. If flow control of source port is enabled, the pause frame is sent out to prohibit more frames from coming in.

3.3 VLAN

The QCA8337N switch supports many VLAN options, including IEEE 802.1q and port-based VLANs. The QCA8337N supports 4096 IEEE 802.1q VLAN groups and 4K VLAN table entries. The QCA8337N device checks VLAN port membership from the translation VID.

Table 3-4 shows the QCA8337N supported 802.1q modes. The port-based VLAN is enabled according to the user-defined port VID value. The QCA8337N supports optional discard of tagged, untagged, and priority tagged frames. The QCA8337N also supports untagging of the VLAN ID for packets going out on untagged ports on a per-port basis. The QCA8337N also supports double tagging frame which is S-Tag and C-Tag. The QCA8337N can lookup the 4K VLAN table by S-Tag or C-Tag, depending on the configuration mode.

There are also 64 entries in VLAN translation table to support the VLAN operation.

3.3.1 Port-based VLAN

The QCA8337N switch supports port-based VLAN functionality used for non-management frames when 802.1q is disabled on the ingress port. When FORCE_PORT_VLAN_EN is enabled, non-management frames conform to port-based configurations even if 802.1q is enabled on the ingress port. Each ingress port contains a register that restricts the output (or egress) ports to which it can send frames. This port-based VLAN register has a field PORT_VID_MEM that contains the port-based setting. If bit[0] of a port's PORT_VID_MEM is set to 1, the port is allowed to send frames to port 0, bit[2] for port 2, and so on. At reset, the PORT_VID_MEM for each port is set to all 1s, except for each port's own bit, which clears to 0. Note that the CPU port is port 0.

3.3.2 802.1q VLANs

The QCA8337N supports a maximum of 4096 entries in the VLAN table. The device supports 4096 VLAN ID, ranging from 0 to 4095. The QCA8337N supports both shared and independent VLAN learning (SVL and IVL). This means that forwarding decisions are based on the frame's destination MAC address, which should be unique among all VLANs.

3.3.3 VLAN security

The QCA8337N checks the ingress packets based on the VLAN operation mode and decide whether to forward or drop the packets. There are two sets of configuration: one is the ingress VLAN mode; another is 802.1q mode. The ingress VLAN mode is for checking whether the ingress frame is tagged or not. The 802.1q mode is for checking if the ingress VID is valid and if the ingress port belongs to the member. [Table 3-3](#) and [Table 3-4](#) show the details.

Table 3-3 Ingress VLAN mode

ING_VLAN_MODE	Frame with tag	Frame with priority tag	Frame without tag
00	Forward	Forward	Forward
01	Forward	Drop	Drop
10	Drop	Forward	Forward
11	Forward	Forward	Forward

Table 3-4 VLAN security

802.1q	VID miss	VLAN member violation	No violation
Secure	Drop	Drop	Forward Use VLAN table result
Check	Drop	Forward Use VLAN table result	Forward Use VLAN table result
Fallback	Forward Use port-based VLAN	Forward Use VLAN table result	Forward Use VLAN table result
Disable	Forward Use port-based VLAN		

3.3.4 Port isolation

When FORCE_PORT_VLAN_EN is enabled on the ingress port, except for VLAN member check, non-management frames conform to port-based VLAN member check.

3.3.5 Leaky VLAN

The QCA8337N supports leaky VLAN to enable specific frames to be forwarded across VLAN boundary. Three types of frames can be leaked across VLAN boundary: unicast, multicast and ARP. Unicast and multicast are port or MAC address based, and ARP is port-based.

3.3.6 VLAN translation

The QCA8337N supports VLAN translation function. The QCA8337N lookups the VLAN translation table when packets arrive at the ingress port and packets transmit at the egress port.

3.3.7 VLAN translation table

The VLAN translation table allows user to modify the CVID and/or SVID, see [Table 3-5](#).

Table 3-5 VLAN translation table

Bits	Name	Description
48	ONE_TO_ONE_MODE	0 = Disable 1:1 VLAN 1 = Enable 1:1 VLAN
47	C_VID_EN	1 = CVID enable
46	S_VID_EN	1 = SVID enable
45	O_VID_C	0 = Use SVID 1 = Use CVID
44:38	PORT_BIT_MAP	Used to source when frame received, destination port when frame send out.
37:36	ENTRY_MODE	00 = Invalid entry 01 = Forward lookup enable (o -> s,c) 10 = Reverse lookup enable (s,c -> o) 11 = Forward & reverse lookup both enabled
35:24	C_VID	Custom VID
23:12	S_VID	Service VID
11:0	O_VID	Original VID

3.3.8 Egress mode

The QCA8337N supports per port egress VLAN mode:

- Tagged
- Untagged
- Unmodified
- Untouched

Frames sent out with tagged or untagged depend on the egress mode setting, see [Table 3-6](#).

Table 3-6 VLAN egress mode — tagging

EG_VLAN_MODE	Egress VID= Untagged	Egress VID = Priority tagged	Egress VID = Tagged
Tagged	Egress port default VID	Egress port default VID	Egress VID
Unmodified	Untagged	Priority untagged	Egress VID
Untagged	Untagged	Untagged	Untagged
Untouched	Original packet's encapsulation		

The egress mode can be defined by the different operation modes, see [Table 3-7](#).

Table 3-7 VLAN egress mode

802.1q disabled on egress port			Port-based egress VLAN mode
Edge port	S-Tag mode		Port-based egress VLAN mode
	C-Tag mode		VLAN-based egress VLAN mode
Core port	S-Tag mode	S-Tag	VLAN-based egress VLAN mode
		C-Tag	Keep translation result
	C-Tag mode	S-Tag	Keep translation result
		C-Tag	VLAN-based egress VLAN mode

3.3.9 VLAN table

The QCA8337N supports 4K VLAN membership table. It also supports the following commands to access the VLAN table.

- Read one entry
- Use Get Next to read out whole table
- Load and purge of an entry
- Flush all entries, flush all of one port's entries

Table 3-8 VLAN table format

Bits	Name	Description
20	VALID	0 = Entry is empty 1 = Entry is valid
19	IVL_EN	0 = VID is used to SVL; VID replaced by 0 when search MAC address. 1 = VID is used to IML
18	LEARN_LOOKUP_DIS	0 = Normal operation about learn and final DP 1 = Not learn and not use ARL table DP to calculate final DP, but use UNI flood DP as ARL DP to calculate DP
17:4	EG_VLAN_MODE	[5:4] for port0, [7:6] for port1 ... [17:16] for port6 00 = Unmodified 01 = Untagged 10 = Tagged 11 = Not member
3	PRI_OVER_EN	Priority overwrite enable 0 = Keep the original VLAN priority 1 = Overwrite the VLAN priority with bits[2:0] of this entry
2:0	PRI	Used as frame's VLAN priority when the PRI_OVER_EN (bit[3]) is set to 1.

3.4 ACL

The QCA8337N supports up to 96 ACL rule table entries. Each rule can support filtering or re-direction of the incoming packets based on the following field in the packet.

- Source MAC address
- Destination MAC address
- VID
- EtherType
- Source IP address
- Destination IP address
- Protocol
- Source TCP/UDP port number
- Destination TCP/UDP port number
- Physical port number
- User-defined window pattern

When the incoming packets match an entry in the rules table, the following action can be taken defined in the result field.

- Change C-Tag or S-Tag
- Drop or redirect the packet
- Configure rate limit based on flow
- Change priority
- Force layer 3 NAT operation

The QCA8337N can bind multiple keys and support up to 2 matches per packet to support different functions such as QoS, forwarding, routing, rate measuring/limiting, etc.

3.4.1 ACL rule

The ACL rule is constructed from a packet pattern, pattern mask and action. The pattern can be defined as MAC layer or layer 3 (IPv4 or IPv6) or user-defined window. The ACL pattern types supported by the QCA8337N are listed in [Table 3-9](#).

Table 3-9 ACL patterns

Value	Description
1	MAC pattern
2	IPv4 pattern
3	IPv6 pattern 1
4	IPv6 pattern 2

Table 3-9 ACL patterns (cont.)

Value	Description
5	IPv6 pattern 3
6	Window pattern
7	Enhanced MAC pattern
0	Invalid pattern

3.4.2 Action definition

The action is taken when the defined pattern is matched.

In the ACL rule matching, the QCA8337N supports two match consolidations. If the key of ingress frame is matched with two entries in the ACL, these two actions consolidate. The basic rule for consolidation is that the first action is the first priority if the related bit is active. If the related bit of the first entry is inactive, the second entry is used. But for ACL_MATCH_INT_EN, ACL_DP_ACT and MIRROR_EN field is the OR operation between two actions.

Table 3-10 Action definition

Bits	Name	Description
80	ACL_MATCH_INT_EN	Generate interrupt
79	ACL_EG_TRNAS_BYPASS	Bypass egress QinQ result
78	ACL_RATE_EN	0 = Not use ACL rate limit 1 = Use ACL rate limit
77:73	ACL_RATE_SEL	Select ACL rate limit (index)
72:70	ACL_DP_ACT	111 = Drop 011 = Redirect 001 = Copy to CPU 000 = Forward
69	MIRROR_EN	1 = Mirror packet to mirror port
68	DES_PORT_OVER_EN	1 = Use DES_PORT to determine packet destination port. It can cross VLAN.
67:61	DES_PORT	If DES_PORT_EN is set to 1, these bits are used to determine destination port.
60	ENQUEUE_PRI_OVER_EN	1 = Use ENQUEUE_PRI to determine enqueue priority
59:57	ENQUEUE_PRI	Enqueue priority
56	ARP_WCMP	1 = Select hash
55:49	ARP_INDEX	Index of ARP table
48	ARP_INDEX_OVER_EN	Overwrite the router's result

Table 3-10 Action definition (cont.)

Bits	Name	Description
47:46	FORCE_L3_MODE	00 = No force 01 = SNAT 10 = DNAT 11 = Reserved
45	LOOKUP_VID_CHANGE_EN	1 = Lookup use VID in S-Tag or C-Tag, determined by switch tag mode. For S-Tag mode, use S-Tag; for C-Tag mode, use C-Tag.
44	TRANS_CTAG_CHANGE_EN	Enqueue egress translation key change enable
43	TRANS_STAG_CHANGE_EN	Enqueue egress translation key change enable
42	CTAG_DEI_CHANGE_EN	1 = Frame should be send out by C-Tag; CFI changed to C-Tag[12]
41	CTAG_PRI_REMAP_EN	1 = Frame should be send out by C-Tag; priority changed to C-Tag[15:13]
40	STAG_DEI_CHANGE_EN	1 = Frame should be send out by S-Tag; CFI changed to S-Tag[12]
39	STAG_PRI_REMAP_EN	1 = Frame should be send out by S-Tag; priority changed to S-Tag[15:13]
38	DSCP_REMAP_EN	Modify the DSCP of packet 0 = Unmodified 1 = Modified
37:32	DSCP	DSCP value
31:16	CTAG	[15:13] C-Tag priority [12] CFI [11:0] C-Tag VID
15:0	STAG	[15:13] S-Tag priority [12] DEI [11:0] S-Tag VID

3.4.3 MAC pattern

The action is taken when the MAC pattern is matched.

Table 3-11 MAC pattern

Byte	Name	Description
16	[7] RULE RESULT INVERSE EN	0 = Apply action on the rule entry matches 1 = Apply action on the rule entry does not match
	[6:0] SOURCE PORT	Enable rule for physical source port
15:14	TYPE	EtherType field
13:12	VLAN[15:13] PRIORITY	VLAN priority bits
	[12] CFI	VLAN CFI bit
	[11:0] VID/VID LOW	This field can be VID or VID_LOW, depending on the VID_MASK_OPTION.

Table 3-11 MAC pattern (cont.)

11:4	SA	Source address
3:0	DA	Destination address

Table 3-12 MAC pattern mask

Byte	Name	Description
16	[7:6] RULE VALID	00 = Start 01 = Continue 10 = End 11 = Start & end
	[5] FRAME WITH TAG MASK	0 = Ignore FRAME_WITH_TAG 1 = Consider FRAME_WITH_TAG
	[4] FRAME_WITH_TAG	0 = Untagged frame 1 = Tagged frame
	[3] VID MASK	0 = Range 1 = Mask
	[2:0] RULE TYPE	These three bits must be 001 to indicate the MAC rule.
15:14	TYPE MASK	Enable check mask for EtherType
13:12	VLAN [15:13] PRIORITY MASK	Enable check mask for VLAN priority
	[12] CFI MASK	Enable check mask for VLAN CFI
	[11:0] VID MASK/VID HIGH	Enable check mask for VID to define VID upper boundary
11:6	SA MASK	Enable check mask for SA
5:0	DA MASK	Enable check mask for DA

3.4.4 IPv4 pattern

The action is taken when the IPv4 rule is matched.

Table 3-13 IPv4 pattern

Byte	Name	Description
16	[7] RULE RESULT INVERSE EN	0 = Apply action on frames that match the rule 1 = Apply action on frames that do not match the rule
	[6:0] SOURCE PORT	Enable rule for physical source port
15	[7:6] RESERVED	
	[5:0] TCP FLAGS	TCP control bits

Table 3-13 IPv4 pattern (cont.)

Byte	Name	Description
14	[7] RESERVED	
	[6] DHCPv4	DHCPv4 frame
	[5] RIPv1	RIPv1 frame
	[4]SPORT_FIELD_TYPE	0 = TCP/UDP sport 1 = ICMP type/code
	[3:0] RESERVED	
13:12	TCP/UDP SOURCE PORT/ TCP/UDP SOURCE PORT LOW OR ICMP TYPE CODE	TCP/UDP source port number or low bound port number. See mask byte 14 bit[0].
11:10	TCP/UDP DESTINATION PORT/ TCP/UDP DESTINATION PORT LOW	TCP/UDP destination port number or low bound port number. See mask byte 14 bit[1].
9	DSCP	DSCP field
8	IP PROTOCOL	IP protocol
7:4	SIP	Source IP address
3:0	DIP	Destination IP address

Table 3-14 IPv4 mask

Byte	Name	Description
16	[7:6] RULE VALID	00 = Start 01 = Continue 10 = End 11 = Start&end
	[5:3] RESERVED	
	[2:0] RULE TYPE	These three bits must be 010 to indicate the IPv4 rule.
15	[7:6] RESERVED	
	[5:0] TCP FLAGS MASK	Enable check mask for TCP control bits
14	[7] RESERVED	
	[6] DHCPV4 MASK	Enable check for DHCPv4 frame
	[5] RIPv1 MASK	Enable check for RIPv4 frame
	[4:2] RESERVED	
	[1] TCP/UDP DESTINATION MASK	Indicates the definition of bytes 11 and 10. 0 = Range 1 = Mask
	[0] TCP/UDP SOURCE MASK	Indicates the definition of bytes 13 and 12. 0 = Range 1 = Mask

Table 3-14 IPv4 mask (cont.)

Byte	Name	Description
13:12	TCP/UDP SOURCE PORT MASK/ TCP/UDP SOURCE PORT HIGH OR ICMP TYPE CODE MASK	This can be mask or high definition. See byte 14, bit[0].
11:10	TCP/UDP DESTINATION PORT MASK/ TCP/UDP DESTINATION PORT HIGH	This can be mask or high definition. See byte 14, bit[1].
9	DSCP MASK	Enable check for DSCP bits
8	IP PROTOCOL MASK	Enable check for IP protocol bits
7:4	SIP MASK	Enable check for SIP
3:0	DIP MASK	Enable check for DIP

3.4.5 IPv6 pattern

Table 3-15 IPv6 pattern 1

Byte	Name	Description
16	[7] RULE RESULT INVERSE EN	0 = Apply action on the rule entry matches 1 = Apply action on the rule entry does not match
	[6:0] SOURCE PORT	Enable rule for physical source port
15:0	DIP	Destination IP address

Table 3-16 IPv6 pattern 2

Byte	Name	Description
16	[7] RULE RESULT INVERSE EN	0 = Apply action on the rule entry matches 1 = Apply action on the rule entry does not match
	[6:0] SOURCE PORT	Enable rule for physical source port
15:0	SIP	Source IP address.

Table 3-17 IPv6 pattern 3

Byte	Name	Description
16	[7] RULE RESULT INVERSE EN	0 = Apply action on the rule entry matches 1 = Apply action on the rule entry does not match
	[6:0] SOURCE PORT	Enable rule for physical source port
15	[7:6] RESERVED	
	[5:0] TCP FLAGS	TCP control bits

Table 3-17 IPv6 pattern 3 (cont.)

14	[7] RESERVED	
	[6] DHCPv6	DHCPv6 frame
	[5] RESERVED	
	[4]SPORT_FIELD_TYPE	0 = TCP/UDP SPORT 1 = ICMP TYPE/CODE
	[3:0] RESERVED	
13:12	TCP/UDP SOURCE PORT/ TCP/UDP SOURCE PORT LOW or ICMP TYPE CODE	TCP/UDP source port number or the low bound port number. See mask byte 14 bit[0]. ICMP type code, see byte 14 bit[4].
11:10	TCP/UDP DESTINATION PORT/ TCP/UDP DESTINATION PORT LOW	TCP/UDP destination port number or the low bound port number, see mask byte 14 bit[1].
9	RESERVED	
8:6	[23:20] RESERVED	
	[19:0] IPV6 FLOW LABEL	IPv6 flow label
5:2	RESERVED	
1	DSCP	DSCP field
0	IP PROTOCOL	IP protocol

Table 3-18 IPv6 Mask 1

Byte	Name	Description
16	[7:6] RULE VALID	00 = Start 01 = Continue 10 = End 11 = Start&end
	[5:3] RESERVED	
	[2:0] RULE TYPE	These three bits must be 011 to indicate the IPv6 rule 1.
15:0	DIP MASK	Enable check for destination IP address

Table 3-19 IPv6 mask 2

Byte	Name	Description
16	[7:6] RULE VALID	00 = Start 01 = Continue 10 = End 11 = Start&end
	[5:3] RESERVED	
	[2:0] RULE TYPE	These three bits must be 100 to indicate the IPv6 rule 2
15:0	SIP MASK	Enable check for source IP address

Table 3-20 IPv6 mask 3

Byte	Name	Description
16	[7:6] RULE VALID	00 = Start 01 = Continue 10 = End 11 = Start&end
	[5:3] RESERVED	
	[2:0] RULE TYPE	These three bits must be 101 to indicate the IPv6 rule 3.
15	[7:6] RESERVED	
	[5:0] TCP FLAGS MASK	Enable check mask for TCP control bits
14	[7] FORWARD TYPE MASK	
	[6] DHCPV6 MASK	Enable check for DHCPv6 frame
	[5] RESERVED	
	[4:2] RESERVED	
	[1] TCP/UDP DESTINATION MASK	0 = Range 1 = Mask
	[0] TCP/UDP SOURCE MASK	0 = Range 1 = Mask
13:12	TCP/UDP SOURCE PORT/ TCP/UDP SOURCE PORT HIGH or ICMP TYPE CODE MASK	Enable check for TCP/IP source port or TCP/UDP source port upper bound; Enable check for ICMP type code.
11:10	TCP/UDP DESTINATION PORT/ TCP/UDP DESTINATION PORT HIGHMASK	Enable check for TCP/UDP destination port or TCP/UDP destination port upper bound.
9	RESERVED	
8:6	[23:20] RESERVED	
	[19:0] IPV6 FLOW LABEL MASK	Enable check for IPv6 flow label
5:2	RESERVED	
1	DSCP MASK	Enable check for DSCP
0	IP PROTOCOL MASK	Enable check for IP protocol

3.4.6 Window pattern

Table 3-21 Window pattern

Byte	Name	Description
------	------	-------------

Table 3-21 Window pattern (cont.)

16	[7] RULE RESULT INVERSE EN	0 = Apply action on frames that match the rule 1 = Apply action on frames that do not match the rule
	[6:0] SOURCE PORT	Enable rule for physical source port
15:0	DATA	Data pattern

Table 3-22 Window pattern mask

Byte	Name	Description
16	[7:6] RULE VALID	00 = Start 01 = Continue 10 = End 11 = Start&end
	[2:0] RULE TYPE	These three bits must be 110 to indicate the window rule.
15:0	DATA MASK	Enable check for data pattern

3.4.7 Enhanced MAC pattern

Table 3-23 Enhanced MAC pattern

Byte	Name	Description
16	[7] RULE RESULT INVERSE EN	0 = Apply action on frames that match the rule 1 = Apply action on frames that do not match the rule
	[6:0] SOURCE PORT	Enable rule for physical source port
15	[7] FRAME WITH STAG MASK	0 = Ignore FRAME_WITH_STAG 1 = Consider FRAME_WITH_STAG
	[6] FRAME_WITH_STAG	0 = Frame without S-Tag 1 = Frame with S-Tag
	[5:2] RESERVED	
	[1] DA_SEL	0 = SA & DA[23:0] 1 = DA & SA[23:0]
	[0] SVID MASK	0 = Range 1 = Mask
14:13	TYPE	EtherType
12:11	CTAG	C-Tag
	[15:13] PRIORITY	Priority
	[12] CFI	CFI bit
	[11:0] VID/VID LOW	VID or VID low bound

Table 3-23 Enhanced MAC pattern (cont.)

Byte	Name	Description
10:9	STAG	S-Tag
	[15:13] PRIORITY	Priority
	[12] CFI	CFI bit
	[11:0] VID/VID LOW	VID or VID low bound
8:6	SA_LOW3/DA_LOW3	SA[23:0] or DA[23:0], see byte 15 bit[1].
5:0	DA/SA	Destination or source address, see byte 15 bit[1]

3.4.8 Enhanced MAC pattern mask

Table 3-24 Enhanced MAC pattern mask

Byte	Name	Description
16	[7:6] RULE VALID	00 = Start 01 = Continue 10 = End 11 = Start&end
	[5] FRAME WITH CTAG MASK	0 = Ignore FRAME_WITH_CTAG 1 = Consider FRAME_WITH_CTAG
	[4] FRAME_WITH_CTAG	0 = Frame without C-Tag 1 = Frame with C-Tag
	[3] CVID MASK	0 = Range 1 = Mask
	[2:0] RULE TYPE	These three bits must be 111 to indicate the enhanced MAC rule.
15	RESERVED	
14:13	TYPE MASK	Enable check for EtherType field
12:11	CTAG MASK	Enable check for C-Tag
	[15:13] PRIORITY MASK	Enable check for priority
	[12] CFI MASK	Enable check for CFI bit
	[11:0] VIDMASK/VID HIGH	Enable check for VID or VID upper bound
	10:9	STAG MASK
[15:13] PRIORITY MASK		Enable check for priority
[12] CFI MASK		Enable check for CFI bit
[11:0] VID MASK/VID HIGH		Enable check for VID or VID upper bound
8:6	SA_LOW3/DA_LOW3 MASK	Enable check for SA[23:0] or DA[23:0]
5:0	DA/SA MASK	Enable check for destination or source address

3.5 IGMP/MLD snooping

The QCA8337N switch supports IPv4 IGMP snooping (v1/v2/v3 supported) and IPv6 MLD snooping. By setting the IGMP_MLD_EN bit in the FRAM_ACK_CTRL0/1 register, the QCA8337N can look inside IPv4 and IPv6 packets and redirect IGMP/MLD frames to the CPU for processing.

The QCA8337N also supports hardware IGMP join and fast leave functions. By setting IGMP_JOIN_EN and IGMP_LEAVE_EN bits in the port control register, the QCA8337N updates the ARL table automatically when the QCA8337N receives IGMP Join or Leave packets, and then forward them to the router port directly in case the CPU is not acting as a router or when enabling multicast VLAN_LEAKY to bypass multicast traffic directly from WAN to LAN.

The hardware join/fast leave supports the following packets:

- IGMPv1 join
- IGMPv2/MLDv1 join/leave
- IGMPv3/MLDv2 report excluding NONE or including NONE

3.5.1 IEEE 802.3 reserved group addresses filtering control

The QCA8337N supports the ability to drop, redirect, copy 802.1D specified reserved group MAC addresses 01-80-C2-00-00-04 to 01-80-C2-00-00-0F by adding the addresses to the ARL table.

3.5.2 802.1x

The QCA8337N supports identifying EAPOL frames by their reserved group addresses. Combined with port security feature, the QCA8337N can implement port-based or MAC-based access control.

3.5.3 Forwarding unknown

The QCA8337N can be configured to prevent the forwarding of unicast frames and multicast frames with unregistered destination MAC address on a per-port basis. This can be done by setting UNI_FLOOD_DP and MULTI_FLOOD_DP where a bit represents a port of the QCA8337N.

3.5.4 MAC limit

The QCA8337N supports MAC limit on a per-port basis or a global basis. When the number of learned MAC address limit is reached, the QCA8337N can be configured to forward a frame with a new source MAC address to the CPU or it can be dropped.

3.6 Atheros header

The QCA8337N support proprietary Qualcomm Atheros header that can indicate the packet information and allow CPU to control the packet forwarding. The header can be 2 bytes or 4 bytes with additional 2 bytes identifier. For 2 bytes header, each packet sent out or received must include header. For 4 bytes header, header can exist only in the management frame and there is no header in the normal frame. The Atheros header also supports read/write register through the CPU port.

Table 3-25 shows the type in the Atheros header.

Table 3-25 Type definition for Atheros header

Type	Packet type	Description
5'h0	NORMAL	Normal packet
5'h1	MIB	The packet includes MIB counter for the source port number in the header.
5'h2	READ_WRITE_REG_ACK	This packet indicates the register data for read register command or acknowledge for write register command. See "Atheros header receive" on page 58.
5'h3	802.1x	802.1x
5'h4	RESERVED MAC ADDR	Reserved ARL
5'h5	RIPv1	RIPv1
5'h6	DHCP	DHCP
5'h7	PPPoE DISCOVERY	PPPoE discovery
5'h8	ARP	ARP (If ARP not found, change this type to 5'h13)
5'h9	RESERVED	Reserved for RARP
5'hA	IGMP	IGMP packets
5'hB	MLD	MLD packets
5'hC	RESERVED	Reserved for neighbor discovery
5'hD	Redirect to CPU	ACL_REDIRECT_TO_CPU, ARL_REDIRECT_TO_CPU offload match redirect to CPU
5'hE	Normalization	The frame does not comply with normal TCP/IP flow.
5'hF	Learn limit	The MAC address reaches the learning limit.
5'h10	IPv4 NAT to CPU	Doing NAT and TCP special status; Doing NAT and frame is IP fragment.
5'h11	IP frame: SIP not found	The SIP in IP frame does not pass the source check.
5'h12	NAT not found	NAT not found
5'h13	ARP not found	The ARP frame does not pass the source check.
5'h14	IP frame: Routing not found	The frame DIP is not found in the routing table.
5'h15	TTL exceed	The router tries to forward one frame, but the TTL is 0 after decrease 1 and the destination is not CPU.
5'h16	MTU exceed	The frame length exceeds the MTU.

Table 3-25 Type definition for Atheros header (cont.)

Type	Packet type	Description
5'h17	Copy to CPU	ACL_COPY_TO_CPU, ARL_COPY_TO_CPU, Offload match copy to CPU
5'h18	Mirror to CPU	ACL_MIRROR_TO_CPU, ARL_MIRROR_TO_CPU, PORT_MIRROR_TO_CPU, Offload match mirror
5'h19	Flooding to CPU	Broadcast flooding to CPU, unknown unicast/multicast flooding to CPU
5'h1A	Forwarding to CPU	Bridging to CPU(ARL DP), routing to CPU (offload match), IGMP hardware join/leave forwarding to CPU, special DIP header/ACL assigned DP

3.6.1 Transmit

The QCA8337N sends out the frame with Atheros header when header is enabled. The header indicates the source port of the frame, frame type and priority. The detailed format of Atheros header is shown in [Table 3-26](#).

Table 3-26 Atheros header transmit format

Bits	Name	Description
15:14	VERSION	The value is 10.
13:11	PRIORITY	Frame priority
10:6	TYPE	Frame type. See "Type definition for Atheros header" on page 57.
5:4	RESERVED	
3	FRAME_WITH_TAG	The ingress frame is tagged.
2:0	SOURCE_PORT_NUM	The ingress port number

3.6.2 Receive

The QCA8337N recognizes the Atheros header on receive when the header is enabled. The format is depicted in [Table 3-27](#).

Table 3-27 Atheros header receive

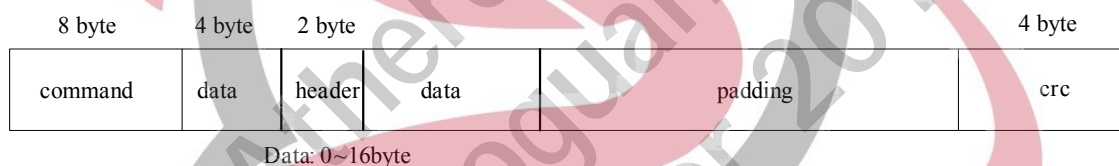
Bit	Name	Description
15:14	VERSION	The version must be 10.
13:11	PRIORITY	Frame priority

Table 3-27 Atheros header receive (cont.)

Bit	Name	Description
10:8	CONTROL	0 = Normal 1 = Read/write register 2 = Disable learn 3 = Disable offload 4 = Disable learn & offload
7	FROM_CPU	The bit indicates the forwarding method. 0 = The forwarding is based on the lookup result. 1 = The forwarding is based on DP_BIT_MAP and bypass lookup.
6:0	DP_BIT_MAP	These bits indicate the forwarding port map. See the description in FROM_CPU.

3.6.3 Header for read/write register

The QCA8337N supports the read/write register through the Atheros header. [Figure 3-1](#) shows the frame format of the read/write register command.

**Figure 3-1 Read/write register command frame format****Table 3-28 Command format for read/write register using Atheros header**

Bit	Name	Description
63:32	SEQ_NUM	The sequence number can be checked by CPU.
31:29	CHECK_CODE	Must be 101, otherwise the command would be ignored.
28	CMD	0 = Write 1 = Read
27:24	RESERVED	
23:20	LENGTH	The data length for read/write register. Maximum is 16 bytes.
18:0	ADDR	The starting register address for the read/write command. The address must be boundary of word address.

3.7 MIB/statistics counters

The statistics counter block maintains a set of forty MIB counters per port. These counters provide a set of Ethernet statistics for frames received on ingress and transmitted on egress. A register interface allows the CPU to capture, read, or clear the counter values.

The counters support:

- RMON MIB
- Ethernet-like MIB
- MIB II
- Bridge MIB
- RFC2819

The CPU interface supports:

- Autocast MIB counters after half-full
- Autocast MIB counters after timeout
- Autocast MIB counters when requested
- Clearing all MIB counters

Table 3-29 describes the statistics counter for each port.

Table 3-29 MIB counters

Counter	Width	Offset	Description
RxBroad	32 bit	0x00	The number of good broadcast frames received
RxPause	32 bit	0x04	The number of pause frames received
RxMulti	32 bit	0x08	The number of good multicast frames received
RxFcsErr	32 bit	0x0c	The total number of frames received with a valid length, but an invalid FCS and an integral number of octets
RxAlignErr	32 bit	0x10	The total number of frames received with a valid length that do not have an integral number of octets and an invalid FCS
RxUndersize	32 bit	0x14	The number of frames received that are less than 64 bytes long and have a good FCS
RxFragment	32 bit	0x18	The number of frames received that are less than 64 bytes long and have a bad FCS
Rx64Byte	32 bit	0x1C	The number of frames received that are exactly 64 bytes long, including those with errors
Rx128Byte	32 bit	0x20	The number of frames received whose length is between 65 and 127 bytes, including those with errors
Rx256Byte	32 bit	0x24	The number of The number of frames received whose length is between 128 and 255 bytes, including those with errors

Table 3-29 MIB counters (cont.)

Counter	Width	Offset	Description
Rx512Byte	32 bit	0x28	The number of frames received whose length is between 256 and 511 bytes, including those with errors
Rx1024Byte	32 bit	0x2C	The number of frames received whose length is between 512 and 1023 bytes, including those with errors
Rx1518Byte	32 bit	0x30	The number of frames received whose length is between 1024 and 1518 bytes, including those with errors
RxMaxByte	32 bit	0x34	The number of frames received whose length is between 1519 and max length, including those with errors (jumbo)
RxTooLong	32 bit	0x38	The number of frames received whose length exceeds max length, including those with FCS errors
RxGoodByte	64 bit	0x3C 0x40	Total data octets received in a frame with a valid FCS. All frame sizes are included.
RXBadByte	64 bit	0x44 0x48	Total data octets received in frame with and invalid FCS. All frame sizes are included. Pause frame is included with a valid FCS
RxOverFlow	32 bit	0x4C	Total valid frames received that are discarded due to lack of buffer space
Filtered	32 bit	0x50	Port disabled and unknown VID
TxBroad	32 bit	0x54	Total good frames transmitted with a broadcast destination address
TxPause	32 bit	0x58	Total good PAUSE frames transmitted
TxMulti	32 bit	0x5C	Total good frames transmitted with a multicast destination address
TxUnderRun	32 bit	0x60	Total valid frames discarded that were not transmitted due to transmit FIFO buffer underflow
Tx64Byte	32 bit	0x64	Total frames transmitted with a length of exactly 64 bytes, including errors
Tx128Byte	32 bit	0x68	Total frames transmitted with a length between 65 and 127 bytes, including those with errors
Tx256Byte	32 bit	0x6C	Total frames truncated with a length between 128 and 255 bytes, including those with errors
Tx512Byte	32 bit	0x70	Total frames truncated with a length between 256 and 511 bytes, including those with errors
Tx1024Byte	32 bit	0x74	Total frames truncated with a length between 512 and 1023 bytes, including those with errors
Tx1518Byte	32 bit	0x78	Total frames transmitted with length between 1024 and 1518, including those with errors (jumbo)
TxMaxByte	32 bit	0x7C	Total frames transmitted with length between 1519 and Maxlength, including those with errors (jumbo)
TxOverSize	32 bit	0x80	Total frames over Maxlength but transmitted truncated with bad FCS
TxByte	64 bit	0x84 0x88	Total data octets transmitted from counted, including those with a bad FCS
TxCollision	32 bit	0x8C	Total collisions experienced by a port during packet transmission
TxAbortCol	32 bit	0x90	Total number of frames not transmitted because the frame experienced 16 transmission attempts and is discarded
TxMultiCol	32 bit	0x94	Total number of successfully transmitted frames that experienced more than one collision

Table 3-29 MIB counters (cont.)

Counter	Width	Offset	Description
TxSingleCol	32 bit	0x98	Total number of successfully transmitted frames that experienced exactly one collision
TxExcDefer	32 bit	0x9C	The number of frames that deferred for an excessive period of time
TxDefer	32 bit	0xA0	Total frames whose transmission was delayed on its first attempt because the medium way is busy
TXLateCol	32 bit	0xA4	Total number of times a collision is detected later than 512 bit times into the transmission of a frame
RXUnicast	32 bit	0xA8	Total number of received good unicast frame
TXUnicast	32 bit	0xAC	Total number of transmitted good unicast frame

3.8 LED control

There are totally six LED control rules. Three of them are used to control the LEDs of PHY 0 to PHY 3. The others are used to control the LEDs of PHY4. Each port has three LEDs. The default behaviors of the LEDs are 1000_link_activity, 100_link_activity and 10_link_activity. The LED output is open-drain output, so two or three of them can be connected together to indicate OR operation of the original LEDs. To achieve this operation, another method is to modify the LED control register. These LEDs also can be individually configured On or Off by register.

Each LED can be controlled by the 16 bits shown in [Table 3-30](#).

Table 3-30 LED control

Bits	Name	Description
15:14	PATTERN_EN	00 = LED always off 01 = LED blinking at 4 Hz 10 = LED always on 11 = LED controlled by the following bits
13	FULL_LIGHT_EN	1 = LED lights when link up in full-duplex
12	HALF_LIGHT_EN	1 = LED lights when link up in half-duplex
11	POWER_ON_LIGHT_EN	1 = Module should enter POWER_ON_RESET status after reset.
10	LINK_1000M_LIGHT_EN	1 = LED lights when link up at 1000 Mbps
9	LINK_100M_LIGHT_EN	1 = LED lights when link up at 100 Mbps
8	LINK_10M_LIGHT_EN	1 = LED lights when link up at 10 Mbps
7	COL_BLINK_EN	1 = LED blinks when collision is detected
6	RESERVED	Must be set to 0.
5	RX_BLINK_EN	1 = LED blinks when receiving frame
4	TX_BLINK_EN	1 = LED blinks when transmitting frame
3	RESERVED	Must be set to 0.

Table 3-30 LED control (cont.)

Bits	Name	Description
2	LINKUP_OVER_EN	0 = RX/TX blinking ignores the LINKUP speed. 1 = RX/TX blinking should check with LINKUP speed, LINKUP LED is ON, allow blinking; otherwise, Off.
1:0	LED_BLINK_FREQ	LED blink frequency select 00 = 2 Hz 01 = 4 Hz 10 = 8 Hz 11 = If link up at 1000Mbps, use 8 Hz. If link up at 100Mbps, use 4 Hz. If link up at 10 Mbps, use 2 Hz.

Table 3-31 LED rule default value

Bits	Name	LED_RULE_0/1	LED_RULE_2/3	LED_RULE_4/5
	Default Value	0xCC35	0xCA35	0xC935
15:14	PATTERN_EN	11	11	11
13	FULL_LIGHT_EN	0	0	0
12	HALF_LIGHT_EN	0	0	0
11	POWER_ON_LIGHT_EN	1	1	1
10	LINK_1000M_LIGHT_EN	1	0	0
9	LINK_100M_LIGHT_EN	0	1	0
8	LINK_10M_LIGHT_EN	0	0	1
7	COL_BLINK_EN	0	0	0
6	RESERVED	0	0	0
5	RX_BLINK_EN	1	1	1
4	TX_BLINK_EN	1	1	1
3	RESERVED	0	0	0
2	LINKUP_OVER_EN	1	1	1
1:0	LED_BLINK_FREQ	01: 4 Hz	01: 4 Hz	01: 4 Hz

3.9 EEPROM programming format

Figure 3-2 shows the EEPROM programming format. Note that the last register should be at address 0, and the LOAD_EEPROM bit is written to 0 to stop loading EEPROM state machine.

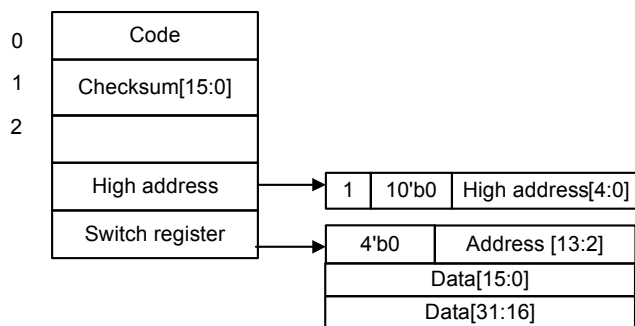


Figure 3-2 EEPROM programming format

3.10 MDC/MDIO access

Figure 3-3 shows the detail format and procedure to access the internal register by MDC/MDIO. Basically, there are two steps to access the register.

- Write the high address. This step can be omitted if the high address is unchanged.
- Read or write the register data. It is allowed to access 16-bit data once instead of twice if the upper or lower 16-bit data is unchanged. When the operation code is 01_B for write operation and 01_B for read operation.

The following describes the detail format used while accessing the registers:

- The first row is the standard format of MDIO access format.
- The second row is the register address of the register A[18:0].
- The third row is the format to write the high address.
- The fourth and fifth rows are the format to read or write data of the register.
- The sixth row shows how to construct the 32 bits data from two 16 bits data.

1. Router uses frame DIP to lookup the ARP table and use the DA in the ARP table to replace the original DA in the frame. Router also replaces the original SA with the router MAC address.
2. NAT replaces the frame SIP and SP with the translation IP and port number in the NAPT table.

DNAT involves the following two steps.

1. NAT replaces the frame DIP and DP with the private IP and private port number in the NAPT table.
2. Router lookups the private IP in ARP table and replaces the DA by the MAC address in the table. Router also replaces the SA with router MAC address.

3.11.1 Basic NAT table

There are 32 entries in the basic NAT table. This table is maintained by CPU only.

Table 3-32 Basic NAT

Bits	Name	Description
99	VALID	0 = Invalid entry 1 = Valid entry
98	PORT NUM EN	Port number compare enable When do SNAT, compare to frame SP When do DNAT, compare to frame DP
97:96	PROTOCOL	Protocol, compare to frame type. 00 = TCP 01 = UDP 10 = GRE 11 = Reserved
95:94	HASHKEY	The value is compared with the hash value generated by the frame's SIP and/or SP depending on the NAT_HASH_MODE.
93:92	ACTION	00 = Mirror 01 = Redirect 10 = Copy 11 = Forward
91	CNT EN	1 = Counter should be add one; counter number selected by CNT INDEX.
90:88	CNT INDEX	Counter index to select entry match.
87:56	PRIVATE IP	12-bit private IP The private IP is constructed under the control bit PRIVATE_IP_BASE_SEL 0 = These 12 bits are the private IP bits[11:0]. 1 = These 12 bits are the private IP bits[19:16] and [7:0]. When do SNAT, compare with frame SIP. When do DNAT, used to change frame DIP.
55:48	RANGE	Port number range. Port number start <= port number < port number start + range

Table 3-32 Basic NAT (cont.)

Bits	Name	Description
47:32	PORT NUM START	Port number start value When do SNAT, compare to frame SP. When do DNAT, compare to frame DP.
31:0	SIP	Router SIP When do SNAT, used to change frame SIP. When do DNAT, compare with frame DIP.

The lookup field depends on the direction of the frame. For the SNAT, the SP, SIP, protocol in the frame is used to match the corresponding field in the table. While doing DNAT, the DP, DIP, and protocol in the frame are used.

3.11.2 NAPT entry

There are 1024 entries in the NAPT table. Each entry is 132 bits wide. The detail format is shown in [Table 3-33](#).

Table 3-33 NAPT entry

Bits	Name	Description
131:128	AGING FLAG	15: Static entry 14–1: Dynamic entry 0: Invalid entry
127:124	RESERVED	
123	CNT EN	1 = Frame matched to this entry should be added to counter selected by CNT INDEX.
122:120	CNT INDEX	Counter index to select counter
119:118	PROTOCOL	00 = TCP 01 = UDP 10 = Reserved 11 = GRE
117:116	ACTION	00 = Mirror 01 = Redirect 10 = Copy 11 = Forward
115:84	SIP	32-bit private SIP The private IP is constructed under the control bit PRIVATE_IP_BASE_SEL 0 = These 12 bits are the private IP bits[11:0]. 1 = These 12 bits are the private IP bits[19:16] and [7:0]. When do SNAT, compare with frame SIP. When do DNAT, frame DIP should be change to these bits.

Table 3-33 NAT entry (cont.)

Bits	Name	Description
83:80	TRANS IP INDEX	Translation IP index in public IP table When do DNAT, compare with frame DIP. Use these bits to select IP address in public IP table. When do SNAT, frame SIP should be change to IP, use these bits to select IP address in public IP table.
79:64	TRANS PORT NUM	Translated port number or Call ID When doing DNAT, compare with frame DP or CALL ID When doing SNAT, frame SP should be change to these bits.
63:48	SP	When doing SNAT, compare with frame SP When doing DNAT, frame DP should be change to these bits
47:32	DP	When doing SNAT, compare with frame DP. When doing DNAT, compare with frame SP.
31:0	DIP	When doing SNAT, compare with frame DIP. When doing DNAT, compare with frame SIP.

3.11.3 Router MAC address

There are eight entries in the router MAC address table. Each entry is 74-bit wide. The detail format is shown in [Table 3-34](#).

Table 3-34 Router MAC address

Bits	Name	Description
73:72	ROUTER_MAC_ACT	00 = Invalid 01 = IPv4 router 10 = IPv6 router 11 = IPv4 & IPv6 router
71:60	VID_HIGH	VID range
59:48	VID_LOW	
47:0	ROUTER MAC ADDR	Router MAC address Note: DA

3.11.4 ARP entry

The HNAT module supports 128 entries in the ARP table. The ARP table can be maintained by CPU. It also can be automatically learned or aged by hardware through monitoring the ARP packets. This table is used for router function. The format of ARP table is shown in [Table 3-35](#).

Table 3-35 ARP entry

Bits	Name	Description
207	IP_VER	
206:204	AGING_FLAG	3'h7: Static 3'h1–3'h6: Valid & dynamic 3'h0: Invalid
203	PPPOE EN	1 = Add or change PPPoE header
202:199	PPPOE INDEX	PPPoE session ID index, for change session or add PPPoE header.
198	CNT EN	1 = Frame that matches this entry should be added to counter
197:194	CNT INDEX	Counter index to select counter.
193:192	ACTION	00 = Mirror 01 = Redirect 10 = Copy 11 = Forward
191	CPU ADDR	1 = This entry is for router address frame should be redirected to CPU. Normal frame, not management
190:188	SPORT NUM	When doing ARP lookup, determine destination port number When doing source check, compare to frame SP.
187:179	VID OFFSET	Offset of VID to VID_LOW, VID_LOW+offset used to change frame VID
178:176	ROUTER MAC INDEX	Index in router MAC table
175:128	MAC ADDR	When doing ARP lookup, used to change frame DA When doing source check, compare to frame SA
127:0	IP ADDR	When doing ARP lookup, compare to frame DIP When doing source check, compare to frame SIP

3.12 IEEE 802.3az and energy efficient Ethernet

IEEE 802.3az provides a mechanism to greatly save the power consumption during data packets burst. The link partners enter low power idle state by sending short refresh signals to maintain the link.

There are two operating states: active state for normal data transfer, and low-power state during data packet bursts.

In the low-power state, the QCA8337N shuts off most of the analog and digital blocks to conserve energy. Due to the bursty traffic nature of Ethernet, system stays in low-power mode for most of the time, thus the power saving can be more than 90%.

At the link start up, both link partners exchange information via auto-negotiation to determine if both parties are capable of entering LPI mode.

Legacy Ethernet products are supported, and this is made transparent to the user.

3.12.1 IEEE 802.3az LPI mode

QCA8337N works in the following modes when 802.3az feature is turned on:

- Active: The regular mode to transfer data
- Sleep: Send special signal to inform remote link of entry into low-power state
- Quiet: No signal transmitted on media. Most of the analog and digital blocks are turned off to reduce energy.
- Refresh: Send periodically special training signal to maintain timing recovery and equalizer coefficients
- Wake: Send special wake-up signal to remote link to inform of the entry back into active.

The QCA8337N supports both 1000BASE-Tx EEE and 1000BASE-T EEE.

100BASE-Tx EEE requires asymmetrical operation, meaning each link partner to enter the LPI mode independent of the other partner.

1000BASE-T EEE requires symmetrical operation, meaning both link partners must enter the LPI mode simultaneously.

Figure 3-4 shows the 802.3az operating power modes—802.3az for the QCA8337N.

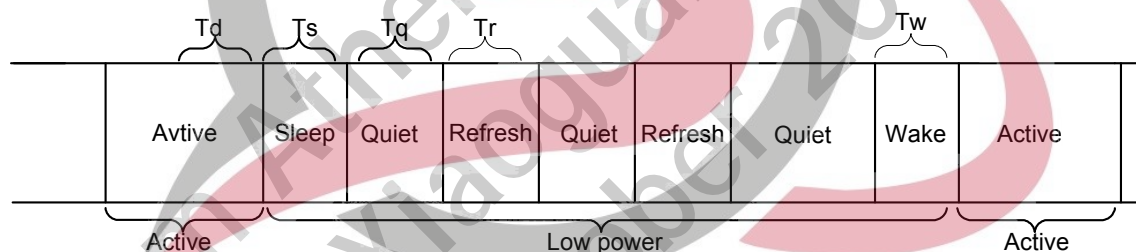


Figure 3-4 Operating power modes—802.3az LPI mode

3.13 Memory map

Table 3-36 Memory map

Register sets	Offset range
Global register	0x00000–0x000FF
EEE register	0x00100–0x00AFF
Parser register	0x00200–0x003FF
ACL register	0x00400–0x005FF
Lookup register	0x00600–0x007FF
QM register	0x00800–0x00BFF
PKT edit register	0x00C00–0x00DFF

Table 3-36 Memory map (cont.)

Register sets	Offset range
Offload register	0x00E00–0x00FFF
Port 0 MIB counter	0x01000–0x010A7
Port 1 MIB counter	0x01100–0x011A7
Port 2 MIB counter	0x01200–0x012A7
Port 3 MIB counter	0x01300–0x013A7
Port 4 MIB counter	0x01400–0x014A7
Port 5 MIB counter	0x01500–0x015A7
Port 6 MIB counter	0x01600–0x016A7
Router MAC	0x02000–0x0207F
Public IP	0x02100–0x021FF
PPPoE session	0x02200–0x022FF
ACL match counter	0x1C000–0x1C0FF
Public IP	0x2A000–0x2A03F
Reserved MAC address	0x3C000–0x3C1FF
ACL rule	0x58000–0x5FFFF
ACL mask	0x59000–0x59FFF
ACL action	0x5A000–0x5A7FF
Public IP	0x5AA00–0x5AAFF
Router MAC	0x5A900–0x5A97F
VLAN translation table	0x5AC00–0x5ADFF
PPPoE session	0x5F000–0x5F03F

4 Electrical Characteristics

4.1 Absolute maximum ratings

Table 4-1 lists the absolute maximum ratings. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 4-1 Absolute maximum ratings

Symbol	Description	Maximum rating	Unit
DVDD	1.2 V digital power supply for core	1.6	V
AVDD	1.2 V analog power supply	1.6	V
DVDD27	2.7 V digital power supply for core	3.0	V
AVDD33	3.3 V analog power supply	4.0	V
T _{store}	Storage temperature	-65 to 150	°C
HBM	ESD human body model	±2	kV
MM	ESD machine model	±200	V
CDM	ESD charge device model	±500	V

4.2 Recommended operating conditions

Table 4-2 lists the recommended operating conditions for the QCA8337N.

Table 4-2 Recommended operating conditions

Symbol	Description	Min	Typ	Max	Unit
DVDD	1.2 V digital power supply for core	1.14	1.20	1.26	V
AVDD	1.2 V analog power supply	1.14	1.20	1.26	V
DVDD27	2.7 V digital power supply for core	2.57	2.70	2.83	V
AVDD33	3.3 V analog power supply	3.14	3.30	3.46	V
T _A	Ambient temperature	–	25	–	°C
T _{J-OPER}	Junction temperature	0	–	120	°C
Ψ _{JT}	Junction to case temperature	–	TBD	–	°C/W

4.3 RGMII/GMII characteristics

Table 4-3 shows the RGMII/GMII DC characteristics.

Table 4-3 RGMII/GMII DC characteristics

Symbol	Parameter	Min	Max	Unit
V_{OH}	Output high level	2.2	-	V
V_{OL}	Output low level	-	0.4	V
I_{IH}	Input high current	-	-0.4	mA
I_{IL}	Input low current	0.4	-	mA
V_{IH}	Input high level	1.7	3.6	V
V_{IL}	Input low level	-	0.7	V

4.4 Power-on strapping

Table 4-4 shows the pin-to-PHY core configuration signal power-on strapping.

Table 4-4 Power-on-strapping

Pin signal	148 pin	Function name	Description
RXD0_0	A55	SPI_EN	0 = No EEPROM connected 1 = EEPROM connected
RXD1_0	B48	SPI_SIZE	0 = 1K 1 = 4K or 2K
RXD2_0	B49	LED_OPEN_EN	0 = Driver 1 = Open drain
RXD3_0	A57	CABLE_DIAG	0 = Disable power on cable diagnostic 1 = Enable power on cable diagnostic
SPI_DO	B43	MDIO_EN	0 = UART interface 1 = MDC/MDIO interface
RXDV_0	A54	CONTROL_DAC_HW0	11 = follow DSP setting (default); the maximum power is high for cable longer than 110 m;
INTn	A80	CONTROL_DAC_HW1	10 = bypass half_amp; set real_half_amp=0; follow DSP half_bias setting. Lose half amplitude capability with short cable and the maximum power is high for cable longer than 100 m; 01 = half amplitude follow DSP, bypass half_bias; set real_half_bias= 1; Use half amplitude capability with short cable and the power is the same for 100m or >110m cable; 00 = everything is full no matter the cable length. This gives the worse power.

Table 4-4 Power-on-strapping (cont.) (cont.)

Pin signal	148 pin	Function name	Description
RXD3_1	A72	PWR_SEL	0 = 1.1 V 1 = 1.2 V
RXD2_1	B61	DISABLE_AZ	0 = Enable az 1 = Disable az

4.4.1 Power-on-reset timing

Figure 4-1 shows the power-on-reset timing diagram.

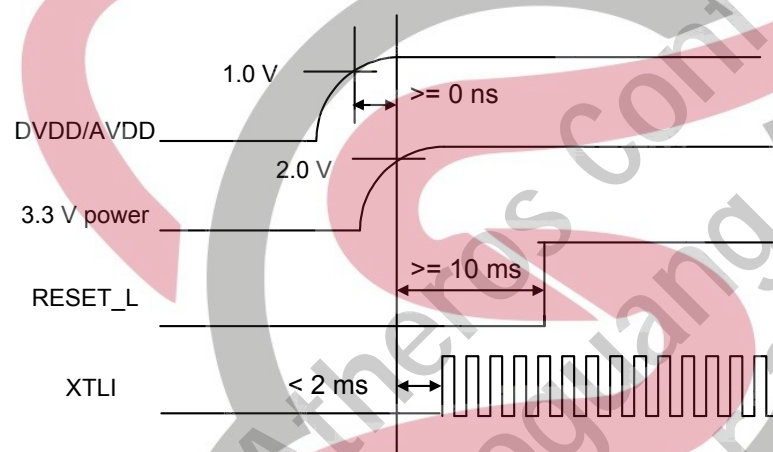


Figure 4-1 Power-on-reset timing diagram

4.5 AC timing

4.5.1 XTAL/OSC timing

Figure 4-2 shows the XTAL timing diagram.

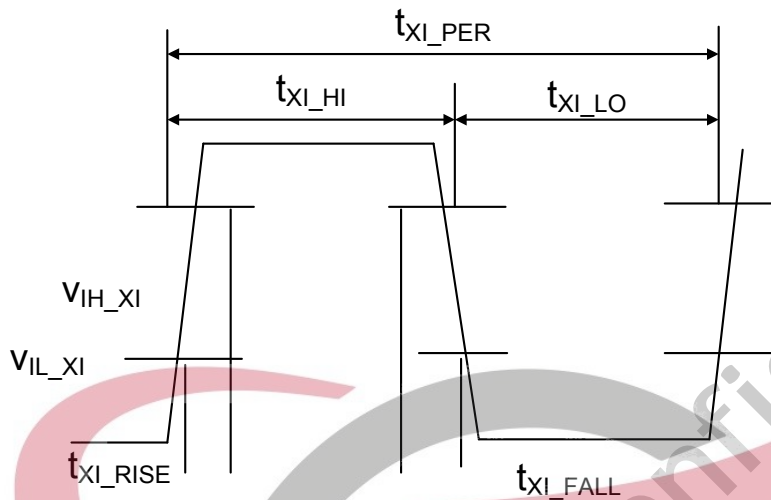


Figure 4-2 XTAL/OSC timing diagram

Table 4-5 XTAL/OSC timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{XI_PER}	XI/OSCI clock period	40.0 - 50ppm	40.0	40.0 + 50ppm	ns
t_{XI_HI}	XI/OSCI clock high	14	20.0	–	ns
t_{XI_LO}	XI/OSCI clock low	14	20.0	–	ns
t_{XI_RISE}	XI/OSCI clock rise time, V_{IL} (max) to V_{IH} (min)	–	–	4	ns
t_{XI_FALL}	XI/OSCI clock fall time, V_{IL} (max) to V_{IH} (min)	–	–	4	ns
V_{IH_XI}	XTLI input high level voltage	0.8	–	1.4	V
V_{IL_XI}	XTLI input low level voltage	-0.3	–	0.15	V

4.5.2 MII timing

Figure 4-3 shows the MII timing diagram.

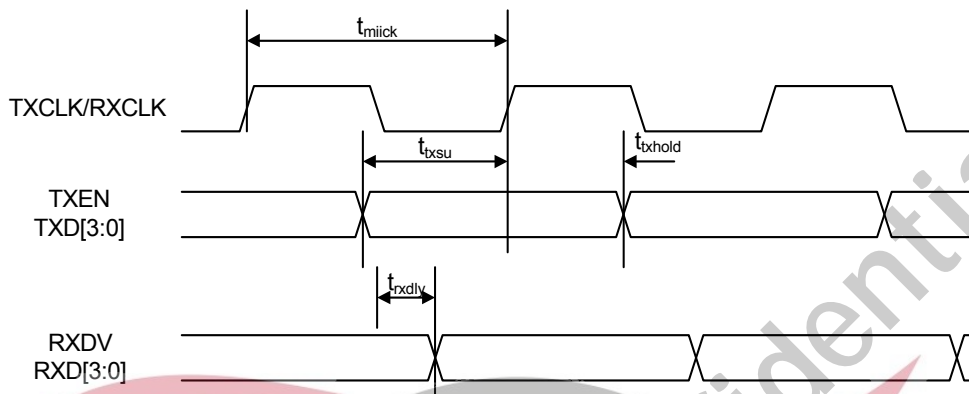


Figure 4-3 MII input timing diagram

Table 4-6 MII timing

Symbol	Parameter	Min	Type	Max	Unit
t_{miick}	TXCLK/RXCLK period	—	40	—	ns
t_{txsu}	TXEN and TXD to TXCLK rising setup	10	—	—	ns
t_{txhold}	TXEN and TXD to TXCLK rising hold	10	—	—	ns
t_{rxdly}	RXCLK falling to RXDV, and RXD output delay	0	—	8	ns

4.5.3 GMII timing

Figure 4-4 shows the GMII timing diagram.

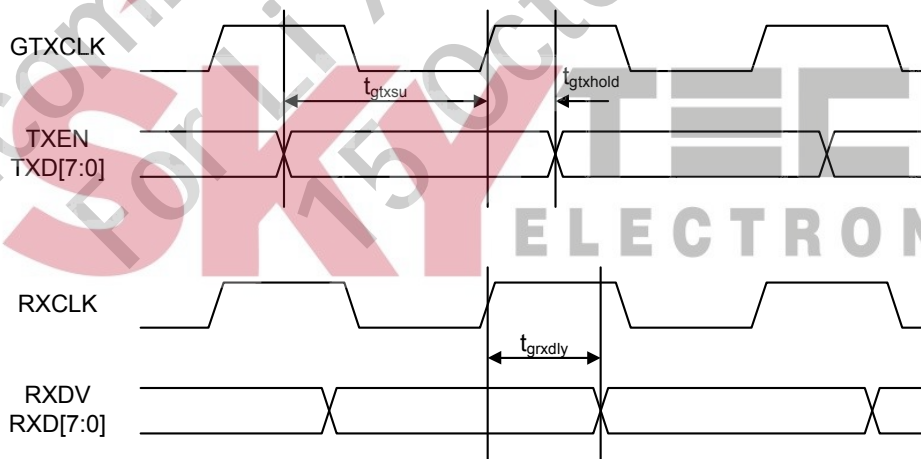


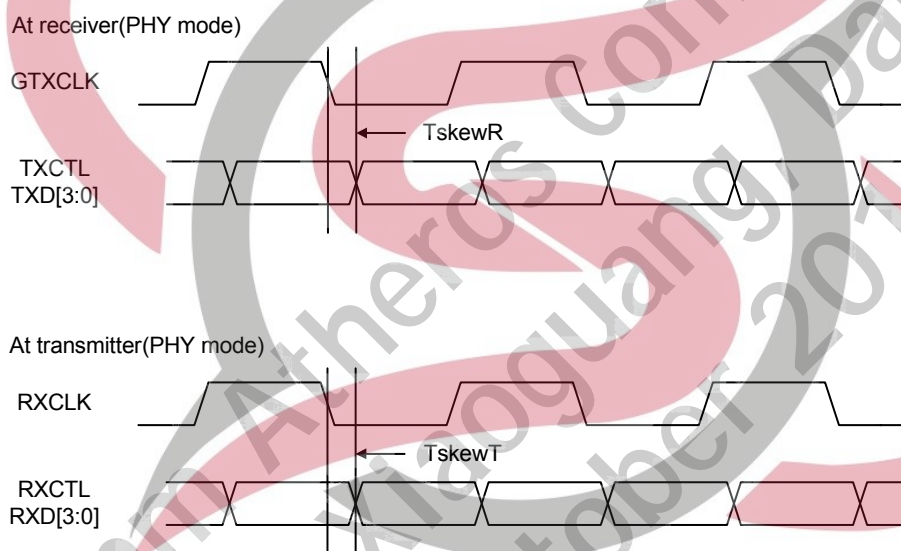
Figure 4-4 1000BASE-T GMII timing diagram

Table 4-7 1000BASE-T GMII timing

Symbol	Parameter	Min	Type	Max	Unit
t_{gtxsu}	TXEN and TXD to GTXCLK	2.0	–	–	ns
t_{gtxhold}	TXEN and TXD GTXCLK rising hold time	0	–	–	ns
t_{grxdly}	RXCLK rising to RXDV, and RXD output delay	0.5	–	5.5	ns

4.5.4 RGMII timing

Figure 4-5 shows the RGMII timing diagram.

**Figure 4-5 RGMII timing diagram****Table 4-8 Reduced GMII timing**

Symbol	Parameter	Min	Typ	Max	Unit
T_{skewT}	Data to clock output skew	-0.5	–	0.5	ns
T_{skewR}	Data to clock input skew	1	–	2.6	ns

4.5.5 SPI timing

Figure 4-6 shows the SPI timing diagram.

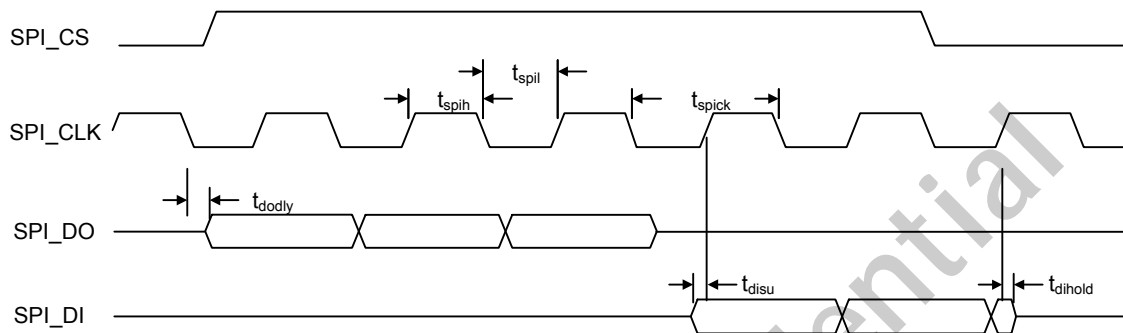


Figure 4-6 EEPROM interface timing diagram

Table 4-9 EEPROM interface timing

Symbol	Parameter	Min	Type	Max	Unit
t _{spick}	SPI_CLK period	-	-	-	ns
t _{spil}	SPI_CLK low period	-	-	-	ns
t _{sph}	SPI_CLK high period	-	-	-	ns
t _{disu}	SPI_DI to SPI_CLK rising setup time	10	-	-	ns
t _{dihold}	SPI_DI to SPI_CLK rising hold time	10	-	-	ns
t _{dodly}	SPI_CLK falling to SPI_DO output delay time	-	-	20	ns

4.5.6 MDIO timing

Figure 4-7 shows the MDIO timing diagram.

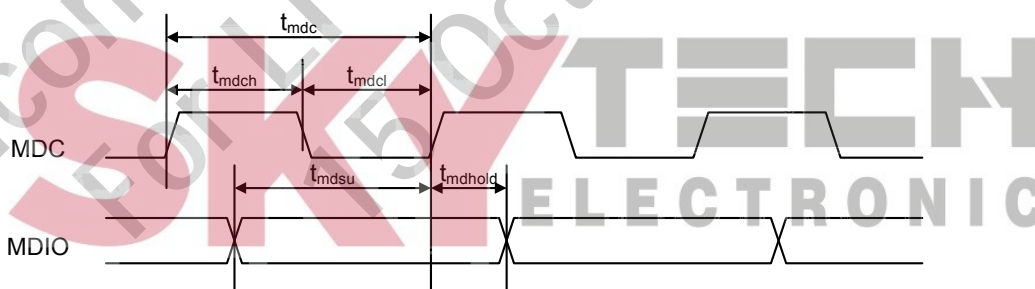


Figure 4-7 MDIO timing diagram

Table 4-10 MDIO timing

Symbol	Parameter	Min	Typ	Max	Unit
t _{mdc}	MDC period	100	-	-	ns
t _{mdcl}	MDC low period	40	-	-	ns

Table 4-10 MDIO timing (cont.)

Symbol	Parameter	Min	Typ	Max	Unit
t_{mdch}	MDC high period	40	–	–	ns
t_{mdsu}	MDIO to MDC rising setup time	10	–	–	ns
t_{mdhold}	MDIO to MDC rising hold time	10	–	–	ns

4.6 Typical power consumption parameters

The following conditions apply to typical characteristics, unless otherwise specified.

- DVDD/AVDD = 1.2 V
- AVDD33 = 3.3 V
- $T_A = 25\text{ }^\circ\text{C}$

Table 4-11 shows typical power drain on each of the on-chip power supply domains as a function of the QCA8337N's operating mode.

Table 4-11 Total system power (1000BASE-T)

Link type	Link status	3.3 V (mA)	1.1 V (mA)	Power consumption (mW)
	No link	TBD	TBD	TBD
1000M	All ports active	TBD	TBD	TBD
	Two ports active	TBD	TBD	TBD
	Three ports active	TBD	TBD	TBD
	Four ports active	TBD	TBD	TBD
100M	All ports active	TBD	TBD	TBD
	Two ports active	TBD	TBD	TBD
	Three ports active	TBD	TBD	TBD
	Four ports active	TBD	TBD	TBD
1000M	All ports 802.3az enabled	TBD	TBD	TBD
100M	All ports 802.3az enabled	TBD	TBD	TBD

5 Register Descriptions

Table 5-1 shows the reset types used in this document.

Table 5-1 Register reset types

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.
Retain	Value written to a register field takes effect without a software reset.
RES	Reserved use. All reserved bits are read as 0, unless otherwise noted.
RO	Read only.
ROC	Read only clear. After a read, the register field is cleared to 0.
R/W	Read/Write
RWC	Read/Write clear on read. All bits are readable and writable. After a reset or after the register is read, the register field is reset to 0.
RWR	Read/Write reset. All bits are readable and writable. After a reset or after the register is read, the register field is cleared to 0.
RWS	Read/Write set. All bits are readable and writable. After a reset, the register field is set to a non-zero value specified in the text.
SC	Self-clear. Write 1 to this register causes the desired function to execute immediately, and the register field clears to 0 when the function is complete.
Update	The value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.
WO	Write only. Read to this type of register field return undefined data.

5.1 Register address space (offset range: 0x0000–0x0E98)

Table 5-2 summarizes address space occupied by the registers.

Table 5-2 Register address space summary

Name	Offset range
Global control register	0x0000–0x00E0
EEE control register	0x0100–0x0168
Parser control register	0x0200–0x0270
ACL control register	0x0400–0x0454
Lookup control register	0x0600–0x0718
QM control register	0x0800–0x0B70
PKT edit control register	0x0C00–0x0C80
Layer 3 control register	0x0E00–0x0E98

5.2 Global control registers (offset range: 0x0000–0x00E0)

Table 5-3 summarizes the global registers.

Table 5-3 Global control registers summary

Name	Offset range
Mask control register	0x0000
Port 0 pad mode control register	0x0004
Port 5 pad mode control register	0x0008
Port 6 pad mode control register	0x000C
Power-on-strapping register	0x0010
Global interrupt register	0x0020–0x0024
Global interrupt mask register	0x0028–0x002C
Module enable control register	0x0030
MIB function register	0x0034
Interface high address register	0x0038
MDIO master control register	0x003C
BIST control register	0x0040
BIST recover register	0x0044
Service tag register	0x0048
LED control register	0x0050–0x005C
Global MAC address	0x0060–0x0064
MAC size register	0x0078
Port0 status register	0x007C
Port1 status register	0x0080
Port2 status register	0x0084

Table 5-3 Global control registers summary (cont.)

Name	Offset range
Port3 status register	0x0088
Port4 status register	0x008C
Port5 status register	0x0090
Port6 status register	0x0094
Header control register	0x0098
Port0 header control register	0x009C
Port1 header control register	0x00A0
Port2 header control register	0x00A4
Port3 header control register	0x00A8
Port4 header control register	0x00AC
Port5 header control register	0x00B0
Port6 header control register	0x00B4
SGMII control register	0x00E0

5.2.1 MASK_CTRL

Address offset: 0x0000

Table 5-4 summarizes the mask control register.

Table 5-4 MASK_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	W/SC	0	SOFT_RET	1 = Software reset This bit is set by the software to initiate the hardware. It is self-cleared by the hardware after the initialization is done.
30:17	RO	0	RESERVED	
16	R/W	0	LOAD_EEPROM	Load EEPROM enable. This bit is set to automatically load registers from EEPROM. It is cleared after the loading is complete.
15:8	RO	0x13	DEVICE_ID	Device identifier
7:0	RO	0x01	REV_ID	Revision identifier

5.2.2 PORT0_PAD_CTRL

Address offset: 0x0004

Table 5-5 summarizes the port 0 pad mode control register.

Table 5-5 PORT0_PAD_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	MAC06_EXCHANGE_EN	Exchange MAC0 and MAC6
30	R/W	0	MAC0_M_RMII_EN	RMII master
29	R/W	0	MAC0_S_RMII_EN	RMII slave
28	R/W	0	MAC0_RMII_SEL	RMII clock inverse
27	R/W	0	MAC0_RMII_PIPE_RXCLK_SEL	
26	R/W	0	MAC0_RGMII_EN	1 = MAC0 connected to CPU through RGMII interface
25	R/W	0	MAC0_RGMII_TXCLK_DELAY_EN	1 = RGMII interface TXCLK (input from CPU) is delayed. Delay value depends on bits[23:22].
24	R/W	0	MAC0_RGMII_RXCLK_DELAY_EN	1 = RGMII interface RXCLK is delayed. 1000M: Delay 2 ns output to CPU 10/100M: Delay value depends on bits[21:20].
23:22	R/W	0	MAC0_RGMII_TXCLK_DELAY_SEL	11–00 Control the delay value of RGMII interface TXCLK. 11 = maximum delay
21:20	R/W	0	MAC0_RGMII_RXCLK_DELAY_SEL	11–00 Control the delay value of RGMII interface RXCLK. 11 = maximum delay
19	R/W	0	SGMII_CLK125M_RX_SEL	Configure the receive clock phase for MAC interface and must be set when using SerDes or SGMII module. 0 = Rising edge 1 = Falling edge
18	R/W	0	SGMII_CLK125M_TX_SEL	Configure the transmit clock phase for SerDes interface 0 = Rising edge 1 = Falling edge
17	R/W	0	FX100_EN	Enable 100BASE-FX interface
16	R/W	0	RESERVED	
15	R/W	0	RESERVED	
14	R/W	0	MAC0_PHY_GMII_EN	1 = MAC0 connected to CPU through GMII interface, PHY mode
13	R/W	0	MAC0_PHY_GMII_TXCLK_SEL	1 = Select invert clock input for port0 PHY mode, GMII interface TXCLK
12	R/W	0	MAC0_PHY_GMII_RXCLK_SEL	1 = Select invert clock output for port0 PHY mode, GMII interface RXCLK
11	R/W	0	MAC0_PHY_MII_PIPE_RXCLK_SEL	1 = Select clock edge for rxpipe; default is invert.
10	R/W	0	MAC0_PHY_MII_EN	1 = MAC0 connected to CPU through MII interface, PHY mode
9	R/W	0	MAC0_PHY_MII_TXCLK_SEL	1 = Select invert clock output for port0 PHY mode, MII interface TXCLK

Table 5-5 PORT0_PAD_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
8	R/W	0	MAC0_PHY_MII_RXCLK_SEL	1 = Select invert clock output for port0 PHY mode, MII interface RXCLK
7	R/W	0	MAC0_SGMII_EN	Enable SGMII interface
6	R/W	0	MAC0_MAC_GMII_EN	1 = MAC0 connected to CPU through GMII interface, MAC mode.
5	R/W	0	MAC0_MAC_GMII_TXCLK_SEL	1 = Select invert clock output for port0 MAC mode, GMII interface TXCLK
4	R/W	0	MAC0_MAC_GMII_RXCLK_SEL	1 = Select invert clock input for port0 MAC mode, GMII interface RXCLK
3	RO	0	RESERVED	
2	R/W	0	MAC0_MAC_MII_EN	1 = MAC0 connected to CPU through MII interface, MAC mode
1	R/W	0	MAC0_MAC_MII_TXCLK_SEL	1 = Select invert clock input for port0 MAC mode, MII interface TXCLK
0	R/W	0	MAC0_MAC_MII_RXCLK_SEL	1 = Select invert clock input for port0 MAC mode, MII interface RXCLK

5.2.3 PORT5_PAD_CTRL

Address offset: 0x0008

Table 5-6 summarizes the port 5 pad mode control register.

Table 5-6 PORT5_PAD_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:27	RO	0	RESERVED	
26	R/W	0	MAC5_RGMII_EN	1 = MAC5 connected to CPU through RGMII interface
25	R/W	0	MAC5_RGMII_TXCLK_DELAY_EN	1 = CPU RGMII interface TXCLK (input from CPU) is delayed. Delay value depends on bits[23:22].
24	R/W	0	MAC5_RGMII_RXCLK_DELAY_EN	1 = RGMII interface RXCLK is delayed. 1000M: Delay 2 ns output to CPU 10/100M: Delay value depends on bits[21:20].
23:22	R/W	0	MAC5_RGMII_TXCLK_DELAY_SEL	11–00 Control the delay value of RGMII interface TXCLK. 11 = maximum delay
21:20	R/W	0	MAC5_RGMII_RXCLK_DELAY_SEL	11–00 Control the delay value of RGMII interface RXCLK. 11 = maximum delay
19:12	RO	0	RESERVED	

Table 5-6 PORT5_PAD_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
11	R/W	0	MAC5_PHY_MII_PIPE_RXCLK_SEL	1 = Select clock edge for rxpipe. Default is invert.
10	R/W	0	MAC5_PHY_MII_EN	1 = MAC5 connected to CPU through MII interface, PHY mode
9	R/W	0	MAC5_PHY_MII_TXCLK_SEL	1 = Select invert clock output for port5 PHY mode, MII interface TXCLK
8	R/W	0	MAC5_PHY_MII_RXCLK_SEL	1 = Select invert clock output for port5 PHY mode, MII interface RXCLK
7:3	R/W	0	RESERVED	
2	R/W	0	MAC5_MAC_MII_EN	1 = MAC5 connected to CPU through MII interface, MAC mode
1	R/W	0	MAC5_MAC_MII_TXCLK_SEL	1 = Select invert clock input for port5 MAC mode, MII interface TXCLK
0	R/W	0	MAC5_MAC_MII_RXCLK_SEL	1 = Select invert clock input for port5 MAC mode, MII interface RXCLK

5.2.4 PORT6_PAD_CTRL

Address offset: 0x000C

Table 5-7 summarizes the port 6 pad mode control register.

Table 5-7 PORT6_PAD_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:27	RO	0	RESERVED	
26	R/W	0	MAC6_RGMII_EN	1 = MAC6 connected to CPU through RGMII interface
25	R/W	0	MAC6_RGMII_TXCLK_DELAY_EN	1 = RGMII interface TXCLK (input from CPU) is delayed. Delay value depends on bits[23:22].
24	R/W	0	MAC6_RGMII_RXCLK_DELAY_EN	1 = RGMII interface RXCLK delay. 1000M: Delay 2 ns output to CPU 10/100M: Delay value depends on bits[21:20].
23:22	R/W	0	MAC6_RGMII_TXCLK_DELAY_SEL	11–00 Control the delay value of RGMII interface TXCLK. 11 = maximum delay
21:20	R/W	0	MAC6_RGMII_RXCLK_DELAY_SEL	11–00 Control the delay value of RGMII interface RXCLK. 11 = maximum delay
19:18	RO	0	RESERVED	
17	R/W	0	PHY4_RGMII_EN	1 = PHY4 connected to CPU through RGMII interface.

Table 5-7 PORT6_PAD_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
16:12	RO	0	RESERVED	
11	R/W	0	MAC6_PHY_MII_PIPE_RXCLK_SEL	1 = Select clock edge for rxpipe. Default is invert.
10	R/W	0	MAC6_PHY_MII_EN	1 = MAC6 connected to CPU through MII interface, PHY mode.
9	R/W	0	MAC6_PHY_MII_TXCLK_SEL	1 = Select invert clock output for port6 PHY mode, MII interface TXCLK.
8	R/W	0	MAC6_PHY_MII_RXCLK_SEL	1 = Select invert clock output for port6 PHY mode, MII interface RXCLK.
7	R/W	0	MAC6_SGMII_EN	
6:3	RO	0	RESERVED	
2	R/W	0	MAC6_MAC_MII_EN	1 = MAC6 connected to CPU through MII interface, MAC mode.
1	R/W	0	MAC6_MAC_MII_TXCLK_SEL	1 = Select invert clock input for port6 MAC mode, MII interface TXCLK.
0	R/W	0	MAC6_MAC_MII_RXCLK_SEL	1 = Select invert clock input for port6 MAC mode, MII interface RXCLK.

5.2.5 PWS_REG

Address offset: 0x0010

Table 5-8 summarizes the power-on-strapping register.

Table 5-8 PWS_REG bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	POWER_ON_SEL	Power-on-strapping select
30:29	RO	0	RESERVED	
28	R/W	0	PACKAGEMIN_EN	1 = Select 88 pins package pinout
27	R/W	0	INPUT_MODE	1 = S17 all GMII interface digital PAD work at input mode
26	R/W	0	RESERVED	
25	R/W	0	SPI_EN_CSR	1 = EEPROM is connected to the switch
24	R/W	0	LED_OPEN_EN_CSR	0 = LED PAD is in driver mode 1 = LED PAD is in open drain mode
23:22	R/W	0	RESERVED	
21	R/W	1	RESERVED	
20:19	R/W	0	RESERVED	
18:17	R/W	1	RESERVED	

Table 5-8 PWS_REG bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
16:13	R/W	0	RESERVED	
12	R/W	1	RESERVED	
11:10	R/W	0	RESERVED	
9:8	R/W	1	RESERVED	
7	R/W	0	SERDES_AEN	SerDes auto-negotiation: 0 = Enable auto-negotiation 1 = Disable auto-negotiation
6	R/W	0	RESERVED	
5	R/W	1	RESERVED	
4:0	R/W	0	RESERVED	

5.2.6 GLOBAL_INT0

Address offset: 0x0020

Table 5-9 summarizes the global interrupt 0 register.

Table 5-9 GLOBAL_INT0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29	R/W1C	0	ACL_INI_INT	Interrupt when ACL memory initial done.
28	R/W1C	0	LOOKUP_INI_INT	Interrupt when address table initial done (including ARL, reserved ARL, VLAN).
27	R/W1C	0	QM_INI_INT	Interrupt when QM memory initial done.
26	R/W1C	0	MIB_INI_INT	Interrupt when MIB memory initial done.
25	R/W1C	0	OFFLOAD_INI_INT	Interrupt when offload memory initial done.
24	R/W1C	0	HARDWARE_INI_DONE	Interrupt when hardware memory initial done.
23	R/W1C	0	ACL_MATCH_INT	Interrupt when ACL match (and ACL_MATCH_INT_EN in ACL result is 1).
22	R/W1C	0	ARL_DONE_INT	Interrupt when address table access is done by CPU.
21	R/W1C	0	ARL_CPU_FULL_INT	Interrupt when CPU loads a new address in address table, but the address's two entries are all valid.
20	R/W1C	0	VT_DONE_INT	VLAN table access is done by CPU.
19	R/W1C	0	MIB_DONE_INT	MIB access done by CPU.
18	R/W1C	0	ACL_DONE_INT	Interrupt when ACL access done by CPU

Table 5-9 GLOBAL_INT0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
17	R/W1C	0	OFFLOAD_DONE_INT	Interrupt when offload table access done by CPU
16	R/W1C	0	OFFLOAD_CPU_FULL_DONE_INT	Interrupt when CPU load a new entry in HNAT table, but the offload's entries are all valid.
15:12	RO	0	RESERVED	
11	R/W1C	0	ARL_LEARN_CREATE_INT	Create new entry. ARL learn a new address: auto learn, add a new address to ARL. IGMP/MLD join a new entry: add new IGMP/MLD multicast entry to ARL
10	R/W1C	0	ARL_LEARN_CHANGE_INT	Change an existing entry. ARL learn: auto learn, address exists. Change to new port IGMP/MLD join new port: add source port to IGMP/MLD multicast entry IGMP/MLD leave port: one port remove from the IGMP/MLD entry
9	R/W1C	0	ARL_DELETE_INT	Delete an existing entry Age: Age one entry from ARL (including UNI/MUL/IGMP...) IGMP/MLD leave port: one IGMP/MLD entry is removed from ARL
8	R/W1C	0	ARL_LEARN_FULL_INT	Interrupt when learn a new address in address table, but the address's two entries are all valid.
7	RO	0	RESERVED	
6	R/W1C	0	NAPT_AGE_DELETE_INT	NAPT age interrupt
5	R/W1C	0	ARP_LEARN_CREATE_INT	Create new entry. ARP learn a new address: auto learn, add a new address to ARP table
4	R/W1C	0	ARP_LEARN_CHANGE_INT	Change an existed entry. ARP learn: auto learn, address exists. Change to new port
3	R/W1C	0	ARP_AGE_DELETE_INT	Interrupt when entry removed by hardware age
2	R/W1C	0	ARP_LEARN_FULL_INT	Interrupt when learning a new address in ARP table, but table is full.
1	R/W1C	0	VT_MISS_VIO_INT	Interrupt when the VID is not in VLAN table.
0	R/W1C	0	VT_MEM_VIO_INT	Interrupt when the VID is in VLAN table, but source port is not the member of the VID.

5.2.7 GLOBAL_INT1

Address offset: 0x0024

Table 5-10 summarizes the global interrupt 1 register.

Table 5-10 GLOBAL_INT1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:20	RO	0	RESERVED	
19	R/W1C	0	THERM_INT	Thermal meter input
18	R/W1C	0	EEPROM_ERR_INT	Interrupt when error occurs during load EEPROM.
17	R/W1C	0	EEPROM_INT	Interrupt when EEPROM load done.
16	R/W1C	0	MDIO_DONE_INT	MDIO access switch register done interrupt
15	R/W1C	0	PHY_INT	Physical layer interrupt
14	R/W1C	0	QM_ERR_INT	Interrupt when QM detect error
13	R/W1C	0	LOOKUP_ERR_INT	Interrupt when lookup detect error
12	R/W1C	0	LOOP_CHECK_INT	Interrupt when loop checked by hardware
11:8	RO	0	RESERVED	
7:1	R/W1C	0	LINK_CHG_INT_EN	Link status change interrupt enable
0	R/W	0	BIST_DONE_INT	Interrupt when BIST done

5.2.8 GLOBAL_INT0_MASK

Address offset: 0x0028

Table 5-11 summarizes the global interrupt 0 mask register.

Table 5-11 GLOBAL_INT0_MASK bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29	R/W	0	ACL_INI_INT_EN	Enable interrupt when ACL memory initial done
28	R/W	0	LOOKUP_INI_INT_EN	Enable interrupt when address table initial done (including ARL, reserved ARL, VLAN).
27	R/W	0	QM_INI_INT_EN	Enable interrupt when QM memory initial done
26	R/W	0	MIB_INI_INT_EN	Enable interrupt when MIB memory initial done
25	R/W	0	OFFLOAD_INI_INT_EN	Enable interrupt when offload memory initial done
24	R/W	0	HARDWARE_INI_DONE_EN	Enable interrupt when hardware memory initial done
23	R/W	0	ACL_MATCH_INT_EN	Enable interrupt when ACL match
22	R/W	0	ARL_DONE_INT_EN	Enable interrupt when address table access is done by CPU
21	R/W	0	ARL_CPU_FULL_INT_EN	Enable interrupt for ARL_CPU_FULL_INT

Table 5-11 GLOBAL_INT0_MASK bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
20	R/W	0	VT_DONE_INT_EN	Enable interrupt for VT_DONE_INT
19	R/W	0	MIB_DONE_INT_EN	Enable interrupt for MIB_DONE_INT
18	R/W	0	ACL_DONE_INT_EN	Enable interrupt for ACL_DONE_INT
17	R/W	0	OFFLOAD_DONE_INT_EN	Enable interrupt for OFFLOAD_DONE_INT
16	R/W	0	OFFLOAD_CPU_FULL_DONE_INT_EN	Enable interrupt for OFFLOAD_CPU_FULL_DONE_INT
15:12	R/W	0	RESERVED	
11	R/W	0	ARL_LEARN_CREATE_INT_EN	Enable interrupt for ARL_LEARN_CREATE_INT
10	R/W	0	ARL_LEARN_CHANGE_INT_EN	Enable interrupt for ARL_LEARN_CHANGE_INT
9	R/W	0	ARL_DELETE_INT_EN	Enable interrupt for ARL_DELETE_INT
8	R/W	0	ARL_LEARN_FULL_INT_EN	Enable interrupt for ARL_LEARN_FULL_INT
7	R/W	0	RESERVED	
6	R/W	0	NAPT_AGE_DELETE_INT_EN	Enable interrupt for NAPT_AGE_DELETE_INT
5	R/W	0	ARP_LEARN_CREATE_INT_EN	Enable interrupt for ARP_LEARN_CREATE_INT
4	R/W	0	ARP_LEARN_CHANGE_INT_EN	Enable interrupt for ARP_LEARN_CHANGE_INT
3	R/W	0	ARP_AGE_DELETE_INT_EN	Enable interrupt for ARP_AGE_DELETE_INT
2	R/W	0	ARP_LEARN_FULL_INT_EN	Enable interrupt for ARP_LEARN_FULL_INT
1	R/W	0	VT_MISS_VIO_INT_EN	Enable interrupt for VT_MISS_VIO_INT
0	R/W	0	VT_MEM_VIO_INT_EN	Enable interrupt for VT_MEM_VIO_INT

5.2.9 GLOBAL_INT1_MASK

Address offset: 0x002C

Table 5-12 summarizes the global interrupt 1 mask register.

Table 5-12 GLOBAL_INT1_MASK bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:20	RO	0	RESERVED	
19	R/W	0	THERM_INT_EN	Thermal meter interrupt enable
18	R/W	0	EEPROM_ERR_INT_EN	Enable interrupt for EEPROM_ERR_INT

Table 5-12 GLOBAL_INT1_MASK bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
17	R/W	0	EEPROM_INT_EN	Enable interrupt for EEPROM_INT
16	R/W	0	MDIO_DONE_INT_EN	Enable interrupt for MDIO_DONE_INT
15	R/W	0	PHY_INT_EN	Enable interrupt for PHY_INT
14	R/W	0	QM_ERR_INT_EN	Enable interrupt for QM_ERR_INT
13	R/W	0	LOOKUP_ERR_INT_EN	Enable interrupt for LOOKUP_ERR_INT
12	R/W	0	LOOP_CHECK_INT_EN	Enable interrupt for LOOP_CHECK_INT
11:1	RO	0	RESERVED	
0	R/W	0	BIST_DONE_INT_EN	Enable interrupt for BIST_DONE_INT

5.2.10 MODULE_EN

Address offset: 0x0030

Table 5-13 summarizes the module enable register.

Table 5-13 MODULE_EN bit description

Bits	R/W	Initial value	Mnemonic	Description
31:10	RO	0	RESERVED	
9	R/W	1	RESERVED	
8	R/W	1	RESERVED	
7:3	R/W	0	RESERVED	
2	R/W	0	L3_EN	1 = Layer 3 offload enable
1	R/W	0	ACL_EN	1 = ACL module enable
0	R/W	0	MIB_EN	0 = MIB count disable 1 = MIB count enable

5.2.11 MIB

Address offset: 0x0034

Table 5-14 summarizes the MIB function register.

Table 5-14 MIB bit description

Bits	R/W	Initial value	Mnemonic	Description
31:27	RO	0	RESERVED	
26:24	R/W	0	MIB_FUNC	000 = No operation 001 = Flush all counters for all ports 010 = Flush all MIB counters of appointed port 011 = Capture all counters for all ports and auto-cast to CPU port 1xx = Reserved
23:21	R/W	0	MIB_FLUSH_PORT	Flush all MIB counters of this port
20	R/W	0	MIB_CPU_KEEP	0 = Clear MIB counter to 0 after read 1 = Do not clear MIB counter after it has been read.
19:18	RO	0	RESERVED	
17	R/W SC	0	MIB_BUSY	0 = MIB module is empty, and can access new command. 1 = MIB module is busy, and can not access another new command.
16	R/W	0	MIB_AT_HALF_EN	MIB auto-cast enable due to half flow. 1 = MIB is auto-cast when any counter's highest bit count to 1.
15:0	R/W	15'h0	MIB_TIMER	MIB auto-cast timer. 0 = MIB does not auto-cast due to timer times out. The time is times of 8.4 ms; recommended value is 'h100.

5.2.12 INTERFACE_HIGH_ADDR

Address offset: 0x0038

Table 5-15 summarizes the interface high address register.

Table 5-15 INTERFACE_HIGH_ADDR bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	SPI_SPEED	0 = Normal operation mode 1 = Fast speed for test
30:28	R/W	0	RESERVED	
27:24	R/W	0xf	RELOAD_TIMER	Reload EEPROM timer If the EEPROM can not be read out, EEPROM is reloaded when the timer done. It's times 8 ms. 0 = No need to reload EEPROM
23:20	R/W	0	RESERVED	

Table 5-15 INTERFACE_HIGH_ADDR bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
19	R/W	0	SGMII_CLK125M_RX_SEL	SGMII interface Rx clock selection 1 = Inverse clock
18	R/W	0	SGMII_CLK125M_TX_SEL	SGMII interface Tx clock selection 1 = Inverse clock
17:10	R/W	0	RESERVED	
9:0	R/W	0	RESERVED	

5.2.13 MDIO master control

Address offset: 0x003C

Table 5-16 summarizes the MDIO master control register.

Table 5-16 MDIO master control bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	MDIO_BUSY	1 = Internal MDIO interface is busy. This bit is set to 1 when CPU read or write PHY register through internal MDIO interface, and is cleared after hardware finish the command.
30	RO	0	MDIO_MASTER_EN	1 = Use MDIO master to configure PHY register. MDC is changed to internal MDC to PHY.
29:28	R/W	0	RESERVED	
27	RO	0	MDIO_CMD	0 = Write 1 = Read
26	R/W	0	MDIO_SUP_PRE	0 = With 32 bits preamble 1 = Suppress preamble enable
25:21	RO	0	PHY_ADDR	PHY address
20:16	R/W	0	REG_ADDR	PHY register address
15:0	R/W	0	MDIO_DATA	When write, these bits are data written to PHY register. When read, these bits are data read out from PHY register.

5.2.14 BIST_CTRL

Address offset: 0x0040

Table 5-17 summarizes the BIST control register.

Table 5-17 BIST_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	BIST_BUSY	This bit is written to 1 to begin BIST test and is cleared to 0 by hardware after test done. 0 = BIST done or idle 1 = BIST test
30	RO	0	BIST_WITH_ONE_ERR	1 = BIST test one error in data memory and can be recovered.
29	RO	0	BIST_PASS	All memory is OK, or only one error in data memory.
28:24	RO	0	RESERVED	
23	R/W	0	BIST_CRITICAL	Enable critical pattern for BIST test
22	R/W	0	BIST_PTN_EN_2	1 = Enable pattern 2 for BIST test
21	R/W	0	BIST_PTN_EN_1	1 = Enable pattern 1 for BIST test
20	R/W	0	BIST_PTN_EN_0	1 = Enable pattern 0 for BIST test
19:0	RO	0	RESERVED	

5.2.15 BIST_RECOVER

Address offset: 0x0044

Table 5-18 summarizes the BIST recover register.

Table 5-18 BIST_RECOVER bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	BIST_RECOVER_EN	1 = Enable hardware recover data memory MBIST error.
30:13	RO	0	RESERVED	
12:0	R/W	0	BIST_RECOVER_ADDR	BIST test error address of memory.

5.2.16 SERVICE_TAG

Address offset: 0x0048

Table 5-19 summarizes the service tag register.

Table 5-19 SERVICE_TAG bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	R/W	0	RESERVED	
17	R/W	0	SWITCH_S-TAG_MODE	Select switch work VLAN mode. 0 = C-Tag mode 1 = S-Tag mode
16	RO	0	RESERVED	
15:0	R/W	0	SERVICE_TAG	These 16 bits are used to identify the service tagged frame when core port is enabled.

5.2.17 LED_CTRL0

Address offset: 0x0050

Table 5-20 summarizes the LED control 0 register.

Table 5-20 LED_CTRL 0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	R/W	0xCC35	LED_CTRL_RULE_1	PHY4 LED0 control rule
15:0	R/W	0xCC35	LED_CTRL_RULE_0	PHY0–PHY3 LED0 control rule

5.2.18 LED_CTRL1

Address offset: 0x0054

Table 5-21 summarizes the LED control 1 register.

Table 5-21 LED_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	R/W	0xCA35	LED_CTRL_RULE_3	PHY4 LED1 control rule
15:0	R/W	0xCA35	LED_CTRL_RULE_2	PHY0–PHY3 LED1 control rule

5.2.19 LED_CTRL2

Address offset: 0x0058

Table 5-22 summarizes the LED control 2 register.

Table 5-22 LED_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	R/W	16'hC935	LED_CTRL_RULE_5	PHY4 LED2 control rule
15:0	R/W	16'hC935	LED_CTRL_RULE_4	PHY0–PHY3 LED2 control rule

5.2.20 LED_CTRL3

Address offset: 0x005C

Table 5-23 summarizes the LED control 3 register.

Table 5-23 LED_CTRL3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:26	R/W	0	RESERVED	
25:24	R/W	11	LED_PATTERN_EN_32	Pattern enable for port3 LED2
23:22	R/W	11	LED_PATTERN_EN_31	Pattern enable for port3 LED1
21:20	R/W	11	LED_PATTERN_EN_30	Pattern enable for port3 LED0
19:18	R/W	11	LED_PATTERN_EN_22	Pattern enable for port2 LED2
17:16	R/W	11	LED_PATTERN_EN_21	Pattern enable for port2 LED1
15:14	R/W	11	LED_PATTERN_EN_20	Pattern enable for port2 LED0
13:12	R/W	11	LED_PATTERN_EN_12	Pattern enable for port1 LED2
11:10	R/W	11	LED_PATTERN_EN_11	Pattern enable for port1 LED1
9:8	R/W	11	LED_PATTERN_EN_10	Pattern enable for port1 LED0
7:2	RO	0	RESERVED	
1:0	R/W	0	BLINK_HIGH_TIME	When LED blinking, these bits determine LED light time. 00 = 50% of blinking period. 250 ms for 2 Hz, 125 ms for 4 Hz, 62.5 ms for 8 Hz. 01 = 12.5% of blinking period 10 = 25% of blinking period 11 = 75% of blinking period

5.2.21 GOL_MAC_ADDR0

Address offset: 0x0060

Table 5-24 summarizes the global MAC address 0 register.

Table 5-24 GOL_MAC_ADDR0 bit description

Bits	RO	Initial value	Mnemonic	Description
31:16	R/W	0	RESERVED	
15:8	R/W	0	MAC_ADDR_BYTE4	Station address of switch, used as source address in pause frame or other management frames.
7:0	R/W	0x01	MAC_ADDR_BYTE5	Station MAC address

5.2.22 GOL_MAC_ADDR1

Address offset: 0x0064

Table 5-25 summarizes the global MAC address 1 register.

Table 5-25 GLOL_MAC_ADDR1 bit description

Bits	RO	Initial value	Mnemonic	Description
31:0	R/W	0	MAC_ADDR_BYTE0	Station MAC address

5.2.23 MAX_FRAME_SIZE

Address offset: 0x0078

Table 5-26 summarizes the maximum frame size register.

Table 5-26 MAX_FRAME_SIZE bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	RO	0	RESERVED	
20	R/W	0	TEST_PAUSE	Test for MAC send out pause frames. MAC sends out pause on frame on positive edge of this signal and pause off frame on negative edge.
19	R/W	0	IPG_DEC_EN	0 = Normal IPG 96 bit time 1 = MAC decreases two bytes of IPG when send out frame and receive check.
18	RO	0	RESERVED	
17	RO	0	RESERVED	
16	R/W	0	MAC_CRC_RESERVE_EN	0 = MAC removes 4 byte CRC when received frame, and add CRC when transmit out frame; 1 = MAC does not remove 4 byte CRC when received frame, and does not add CRC when transmit out frame.

Table 5-26 MAX_FRAME_SIZE bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
15:14	RO	0	RESERVED	
13:0	R/W	'H5EE	MAX_FRAME_SIZE	Maximum frame size can be received and transmitted by MAC. If a packet's size is larger than MAX_FRAME_SIZE, it is dropped by MAC. The value is for normal packet, it is added 4 by MAC if support VLAN, added 8 for double VLAN, and added 2 for Atheros header.

5.2.24 PORT0_STATUS

Address offset: 0x007C

Table 5-27 summarizes the port 0 status register.

Table 5-27 PORT0_STATUS bit description

Bits	R/W	Initial value	Mnemonic	Description
31:13	RO	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_0	PHY link mode enable 0 = MAC can be configured by software. 1 = Enable MAC flow control configure auto-negotiation with PHY
11	RO	0	AUTO_RX_FLOW_EN_0	Transmit flow control enable after auto-negotiation.
10	RO	0	AUTO_TX_FLOW_EN_0	Transmit flow control enable after auto-negotiation.
9	R/W	0	LINK_EN_0	PHY link mode enable 0 = MAC can be configured by software 1 = Enable MAC auto-negotiation with PHY
8	RO	0	LINK_0	Link status: 0 = PHY link down 1 = PHY link up
7	R/W	0	TX_HALF_FLOW_EN_0	1 = Transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_0	Duplex mode: 0 = Half-duplex mode 1 = Full-duplex mode
5	R/W	0	RX_FLOW_EN_0	Rx MAC flow control enable
4	R/W	0	TX_FLOW_EN_0	Tx MAC flow control enable
3	RO	0	RXMAC_EN_0	Rx MAC enable

Table 5-27 PORT0_STATUS bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
2	R/W	0	TXMAC_EN_0	Tx MAC enable
1:0	R/W	0	SPEED_0	Speed mode: 00 = 10M 01 = 100M 10 = 1000M 11 = Error speed mode

5.2.25 PORT1_STATUS

Address offset: 0x0080

Table 5-28 summarizes the port 1 status register.

Table 5-28 PORT1_STATUS bit description

Bits	R/W	Initial value	Mnemonic	Description
31:13	RO	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_1	PHY link mode enable 0 = MAC can be configured by software. 1 = Enable MAC flow control configure auto-negotiation with PHY
11	RO	0	AUTO_RX_FLOW_EN_1	Transmit flow control enable after auto-negotiation.
10	RO	0	AUTO_TX_FLOW_EN_1	Transmit flow control enable after auto-negotiation.
9	R/W	0	LINK_EN_1	PHY link mode enable 0 = MAC can be configured by software. 1 = Enable MAC auto-negotiation with PHY
8	RO	0	LINK_1	Link status: 1 = PHY link up 0 = PHY link down
7	R/W	0	TX_HALF_FLOW_EN_1	1 = Transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_1	Duplex mode: 0 = Half-duplex mode 1 = Full-duplex mode
5	R/W	0	RX_FLOW_EN_1	Rx MAC flow control enable
4	R/W	0	TX_FLOW_EN_1	Tx MAC flow control enable
3	RO	0	RXMAC_EN_1	Rx MAC enable

Table 5-28 PORT1_STATUS bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
2	R/W	0	TXMAC_EN_1	Tx MAC enable
1:0	R/W	0	SPEED_1	Speed mode: 00 = 10M 01 = 100M 10 = 1000M 11 = Error speed mode

5.2.26 PORT2_STATUS

Address offset: 0x0084

Table 5-29 summarizes the port 2 status register.

Table 5-29 PORT2_STATUS bit description

Bits	R/W	Initial value	Mnemonic	Description
31:13	RO	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_2	PHY link mode enable 0 = MAC can be configured by software. 1 = Enable MAC flow control configure auto-negotiation with PHY
11	RO	0	AUTO_RX_FLOW_EN_2	Transmit flow control enable after auto-negotiation.
10	RO	0	AUTO_TX_FLOW_EN_2	Transmit flow control enable after auto-negotiation.
9	R/W	0	LINK_EN_2	PHY link mode enable. 0 = MAC can be configure by software. 1 = Enable MAC auto-negotiation with PHY
8	RO	0	LINK_2	Link status: 1 = PHY link up 0 = PHY link down
7	R/W	0	TX_HALF_FLOW_EN_2	1 = Transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_4	Duplex mode 0 = Half-duplex mode 1 = Full-duplex mode
5	R/W	0	RX_FLOW_EN_2	Rx MAC flow control enable
4	R/W	0	TX_FLOW_EN_2	Tx MAC flow control enable
3	RO	0	RXMAC_EN_2	Rx MAC enable

Table 5-29 PORT2_STATUS bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
2	R/W	0	TXMAC_EN_2	Tx MAC enable
1:0	R/W	0	SPEED_2	Speed mode: 00 = 10M 01 = 100M 10 = 1000M 11 = Error speed mode

5.2.27 PORT3_STATUS

Address offset: 0x0088

Table 5-30 summarizes the port 3 status register.

Table 5-30 PORT 3_STATUS bit description

Bits	R/W	Initial value	Mnemonic	Description
31:13	RO	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_3	PHY link mode enable 0 = MAC can be configured by software. 1 = Enable MAC flow control configure auto-negotiation with PHY
11	RO	0	AUTO_RX_FLOW_EN_3	Transmit flow control enable after auto-negotiation.
10	RO	0	AUTO_TX_FLOW_EN_3	Transmit flow control enable after auto-negotiation.
9	R/W	0	LINK_EN_3	PHY link mode enable 0 = MAC can be configure by software. 1 = Enable MAC auto-negotiation with PHY
8	RO	0	LINK_3	Link status: 0 = PHY link down 1 = PHY link up
7	R/W	0	TX_HALF_FLOW_EN_3	1 = Transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_3	Duplex mode: 0 = Half-duplex mode 1 = Full-duplex mode
5	R/W	0	RX_FLOW_EN_3	Rx MAC flow control enable
4	R/W	0	TX_FLOW_EN_3	Tx MAC flow control enable
3	RO	0	RXMAC_EN_3	Rx MAC enable

Table 5-30 PORT 3_STATUS bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
2	R/W	0	TXMAC_EN_3	Tx MAC enable
1:0	R/W	0	SPEED_3	Speed mode: 00 = 10M 01 = 100M 10 = 1000M 11 = Error speed mode

5.2.28 PORT4_STATUS

Address offset: 0x008C

Table 5-31 summarizes the port 4 status register.

Table 5-31 PORT4_STATUS bit description

Bits	R/W	Initial value	Mnemonic	Description
31:13	RO	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_4	PHY link mode enable 0 = MAC can be configured by software. 1 = Enable MAC flow control configure auto-negotiation with PHY
11	RO	0	AUTO_RX_FLOW_EN_4	Transmit flow control enable after auto-negotiation.
10	RO	0	AUTO_TX_FLOW_EN_4	Transmit flow control enable after auto-negotiation.
9	R/W	0	LINK_EN_4	PHY link mode enable 0 = MAC can be configured by software. 1 = Enable MAC auto-negotiation with PHY
8	RO	0	LINK_4	Link status: 0 = PHY link down 1 = PHY link up
7	R/W	0	TX_HALF_FLOW_EN_4	1 = Transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_4	Duplex mode: 0 = Half-duplex mode 1 = Full-duplex mode
5	R/W	0	RX_FLOW_EN_4	Rx MAC flow control enable
4	R/W	0	TX_FLOW_EN_4	Tx MAC flow control enable
3	RO	0	RXMAC_EN_4	Rx MAC enable

Table 5-31 PORT4_STATUS bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
2	R/W	0	TXMAC_EN_4	Tx MAC enable
1:0	R/W	0	SPEED_4	Speed mode: 00 = 10M 01 = 100M 10 = 1000M 11 = Error speed mode

5.2.29 PORT5_STATUS

Address offset: 0x0090

Table 5-32 summarizes the port 5 status register.

Table 5-32 PORT 5_STATUS bit description

Bits	R/W	Initial value	Mnemonic	Description
31:13	RO	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_5	PHY link mode enable 0 = MAC can be configured by software. 1 = Enable MAC flow control configure auto-negotiation with PHY
11	RO	0	AUTO_RX_FLOW_EN_5	Transmit flow control enable after auto-negotiation.
10	RO	0	AUTO_TX_FLOW_EN_5	Transmit flow control enable after auto-negotiation.
9	R/W	0	LINK_EN_5	PHY link mode enable 0 = MAC can be configure by software. 1 = Enable MAC auto-negotiation with PHY
8	RO	0	LINK_5	Link status 0 = PHY link down 1 = PHY link up
7	R/W	0	TX_HALF_FLOW_EN_5	1 = Transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_5	Duplex mode 0 = Half-duplex mode 1 = Full-duplex mode
5	R/W	0	RX_FLOW_EN_5	Rx MAC flow control enable
4	R/W	0	TX_FLOW_EN_5	Tx MAC flow control enable
3	RO	0	RXMAC_EN_5	Rx MAC enable

Table 5-32 PORT 5_STATUS bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
2	R/W	0	TXMAC_EN_5	Tx MAC enable
1:0	R/W	0	SPEED_5	Speed mode: 00 = 10M 01 = 100M 10 = 1000M 11 = Error speed mode

5.2.30 PORT6_STATUS

Address offset: 0x0094

Table 5-33 summarizes the port 6 status register.

Table 5-33 PORT 6_STATUS bit description

Bits	R/W	Initial value	Mnemonic	Description
31:13	RO	0	RESERVED	
12	R/W	0	FLOW_LINK_EN_6	PHY link mode enable 0 = MAC can be configured by software. 1 = Enable MAC flow control configure auto-negotiation with PHY
11	RO	0	AUTO_RX_FLOW_EN_6	Transmit flow control enable after auto-negotiation.
10	RO	0	AUTO_TX_FLOW_EN_6	Transmit flow control enable after auto-negotiation.
9	R/W	0	LINK_EN_6	PHY link mode enable 0 = MAC can be configure by software. 1 = Enable MAC auto-negotiation with PHY
8	RO	0	LINK_6	Link status: 0 = PHY link down 1 = PHY link up
7	R/W	0	TX_HALF_FLOW_EN_6	1 = Transmit flow control enable in half-duplex mode.
6	R/W	0	DUPLEX_MODE_6	Duplex mode: 0 = Half-duplex mode 1 = Full-duplex mode
5	R/W	0	RX_FLOW_EN_6	Rx MAC flow control enable
4	R/W	0	TX_FLOW_EN_6	Tx MAC flow control enable
3	RO	0	RXMAC_EN_6	Rx MAC enable.

Table 5-33 PORT 6_STATUS bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
2	R/W	0	TXMAC_EN_6	Tx MAC enable
1:0	R/W	0	SPEED_6	Speed mode: 00 = 10M 01 = 100M 10 = 1000M 11 = Error speed mode

5.2.31 HEADER_CTRL

Address offset: 0x0098

Table 5-34 summarizes the header control register.

Table 5-34 HEADER_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:17	RO	0	RESERVED	
16	R/W	0	HEADER_LENGTH_SEL	0 = 2-byte header 1 = 4-byte header
15:0	R/W	0	HEADER_TYPE_VALUE	2-byte header type added between SA & header field

5.2.32 PORT0_HEADER_CTRL

Address offset: 0x009C

Table 5-35 summarizes the port 0 header control register.

Table 5-35 PORT_HEADER_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:6	RO	0	RESERVED	
5	R/W	0	IPG_DEC_EN_0	0 = Normal IPG 96 bit time 1 = MAC decreases two bytes of IPG when send out frame and receive check.
4	R/W	0	MAC_LOOP_BACK_0	1 = Enable MAC loop back at GMII/MII interface

Table 5-35 PORT_HEADER_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
3:2	R/W	0	RX_HEADER_MODE_0	0x0 = No header; 0x1 = Only management with header, must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved
1:0	R/W	0	TX_HEADER_MODE_0	0x0 = No header; 0x1 = Only management with header, must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved

5.2.33 PORT1_HEADER_CTRL

Address offset: 0x00A0

Table 5-36 summarizes the port 1 header control register.

Table 5-36 PORT1_HEADER_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:6	RO	0	RESERVED	
5	R/W	0	IPG_DEC_EN_1	0 = Normal IPG 96 bit time 1 = MAC decreases two bytes of IPG when send out frame and receive check.
4	R/W	0	MAC_LOOP_BACK_1	1 = Enable MAC loop back at GMII/MII interface
3:2	R/W	0	RX_HEADER_MODE_1	0x0 = No header; 0x1 = Only management with header, must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved
1:0	R/W	0	TX_HEADER_MODE_1	0x0 = No header; 0x1 = Only management with header, must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved

5.2.34 PORT2_HEADER_CTRL

Address offset: 0x00A4

Table 5-37 summarizes the port 2 header control register.

Table 5-37 PORT 2_HEADER_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:6	RO	0	RESERVED	
5	R/W	0	IPG_DEC_EN_2	0 = Normal IPG 96 bit time 1 = MAC decreases two bytes of IPG when send out frame and receive check.
4	R/W	0	MAC_LOOP_BACK_2	1 = Enable MAC loop back at GMII/MII interface
3:2	R/W	0	RX_HEADER_MODE_2	0x0 = No header; 0x1 = Only management with header, must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved
1:0	R/W	0	TX_HEADER_MODE_2	0x0 = No header; 0x1 = Only management with header; must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved

5.2.35 PORT3_HEADER_CTRL

Address offset: 0x00A8

Table 5-38 summarizes the port 3 header control register.

Table 5-38 PORT3_HEADER_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:6	RO	0	RESERVED	
5	R/W	0	IPG_DEC_EN_3	0 = Normal IPG 96 bit time 1 = MAC decreases two bytes of IPG when send out frame and receive check.
4	R/W	0	MAC_LOOP_BACK_3	1 = Enable MAC loop back at GMII/MII interface
3:2	R/W	0	RX_HEADER_MODE_3	0x0 = No header; 0x1 = Only management with header, must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved
1:0	R/W	0	TX_HEADER_MODE_3	0x0 = No header; 0x1 = Only management with header; must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved

5.2.36 PORT4_HEADER_CTRL

Address offset: 0x00AC

Table 5-39 summarizes the port 4 header control register.

Table 5-39 PORT4_HEADER_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:6	RO	0	RESERVED	
5	R/W	0	IPG_DEC_EN_4	0 = Normal IPG 96 bit time 1 = MAC decreases two bytes of IPG when send out frame and receive check.
4	R/W	0	MAC_LOOP_BACK_4	1 = Enable MAC loop back at GMII/MII interface
3:2	R/W	0	RX_HEADER_MODE_4	0x0 = No header; 0x1 = Only management with header, must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved
1:0	R/W	0	TX_HEADER_MODE_4	0x0 = No header; 0x1 = Only management with header, must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved

5.2.37 PORT5_HEADER_CTRL

Address offset: 0x00B0

Table 5-40 summarizes the port 5 header control register.

Table 5-40 PORT5_HEADER_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:6	RO	0	RESERVED	
5	R/W	0	IPG_DEC_EN_5	0 = Normal IPG 96 bit time 1 = MAC decreases two bytes of IPG when send out frame and receive check.
4	R/W	0	MAC_LOOP_BACK_5	1 = Enable MAC loop back at GMII/MII interface

Table 5-40 PORT5_HEADER_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
3:2	R/W	0	RX_HEADER_MODE_5	0x0 = No header; 0x1 = Only management with header, must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved
1:0	R/W	0	TX_HEADER_MODE_5	0x0 = No header; 0x1 = Only management with header; must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved

5.2.38 PORT6_HEADER_CTRL

Address offset: 0x00B4

Table 5-41 summarizes the port 6 header control register.

Table 5-41 PORT6_HEADER_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:6	RO	0	RESERVED	
5	R/W	0	IPG_DEC_EN_6	0 = Normal IPG 96 bit time 1 = MAC decreases two bytes of IPG when send out frame and receive check.
4	R/W	0	MAC_LOOP_BACK_6	1 = Enable MAC loop back at GMII/MII interface
3:2	R/W	0	RX_HEADER_MODE_6	0x0 = No header; 0x1 = Only management with header, must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved
1:0	R/W	0	TX_HEADER_MODE_6	0x0 = No header; 0x1 = Only management with header; must be under 4 bytes header mode. 0x2 = All frame with header; 0x3 = Reserved

5.2.39 SGMII_CTRL

Address offset: 0x00E0

Table 5-42 summarizes the SGMII control register.

Table 5-42 SGMII_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	1	FULL_DUPLEX_25M	Full-duplex in the base-page of base-x for auto-negotiation.
30	R/W	1	HALF_DUPLEX_25M	Half-duplex in the base-page of base-x for auto-negotiation.
29:28	R/W	00	REMOTE_FAULT_25M	REMOTE_FAULT[1:0] in the base-page of base-x for auto-negotiation. Generated by the remote_fault logic internal MAC.
27	R/W	0	NEXT_PAGE_25M	NEXT_PAGE index in the base-page of base-x and SGMII PHY/MAC for auto-negotiation.
26	R/W	1	PAUSE_25M	Pause in the base-page of base-x and SGMII-PHY/MAC for auto-negotiation. This part is not included in the standard for SGMII.
25	R/W	1	ASYM_PAUSE_25M	ASYM_PAUSE in the base-page of base-x and SGMII-PHY/MAC for auto-negotiation. This part is not included in the standard for SGMII.
24	R/W	1	PAUSE_SG_TX_EN_25M	Enable transmitting pause in the base-page of base-x and SGMII-PHY/MAC for auto-negotiation.
23:22	R/W	0	MODE_CTRL_25M	MODE_CTRL signal for mode selection among BASE-X (2'h0), SGMII-PHY (2'h1), and SGMII-MAC (2'h2).
21	R/W	0	MR_LOOPBACK, FORCE_SPEED	Indicate loopback from MII register of cooper PHY and force speed control signal.
20	R/W	0	MR_REG4_CH_25M	Indicate register 4 has changed.
19	R/W	0	AUTO_LPI_25M	When RX_LPI_ACTIVE active for once, the register latches this to indicate that the link-partner.
18	R/W	0	PRBS_EN	Enable SerDes PRBS test function.
17	R/W	0	SGMII_TH_LOS[1]	Combined with bit[15], Signal detection threshold setting control 00 = Default 01 = -2dB 10 = +2dB 11 = +2dB
16	R/W	1	DIS_AUTO_LPI_25M	Disable the auto-detect link-partner's az ability.
15	R/W	0	SGMII_TH_LOS[0]	Same as bit[17]
14:13	R/W	11	SGMII_CDR_BW	CDR digital accumulator length control 00 = 0 01 = ±2 10 = ±4 11 = ±8

Table 5-42 SGMII_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
12:10	R/W	001	SGMII_TXDR_CTRL	Default value is 001. 000 = Driver output Vdiff,pp=500 mV 001 = 600 mV 010 = 700 mV 011 = 800 mV 100 = 900 mV 101 = 1 V 110 = 1.1V 111 = 1.2 V
9:8	R/W	0	SGMII_FIBER_MODE	00 = Not in fiber mode 01 = Reserved 10 = Reserved 11 = 1000BASE-FX mode
7	R/W	1	SGMII_SEL_CLK125M	0 = sgmiiclk125m_rx_delay is not delayed 1 = sgmiiclk125m_rx_delay is delayed by 2 ns
6	R/W	1	SGMII_PLL_BW	0 = SGMII PLL bandwidth is low 1 = SGMII PLL bandwidth is high (default)
5	R/W	0	SGMII_HALFTX	0 = TX driver amplitude is normal (default) 1 = TX driver amplitude is half
4	R/W	0	SGMII_EN_SD	0 = Signal detection disabled and SGMII_FB_SDO = 0 1 = Signal detection enabled
3	R/W	0	SGMII_EN_TX	0 = TX driver is in idle and kept in 900 mV 1 = TX driver enabled
2	R/W	0	SGMII_EN_RX	0 = RX chain disabled, CLK125M_RX and DOUT_RX could be any logic of 1 or 0 1 = RX chain enabled
1	R/W	0	SGMII_EN_PLL	0 = SGMII PLL disabled 1 = DSGMII PLL enabled
0	R/W	0	SGMII_EN_LCKDT	0 = Disabled (default) 1 = SGMII VCO control voltage detector and lock detector enabled

5.3 EEE control registers (offset range: 0x0100–0x0168)

Table 5-43 summarizes the EEE control registers.

Table 5-43 EEE control register summary

Name	Offset range
EEE control register	0x0100
Port1 EEE variable register	0x0120–0x0128
Port2 EEE variable register	0x0130–0x0018
Port3 EEE variable register	0x0140–0x0148
Port4 EEE variable register	0x0150–0x0158
Port5 EEE variable register	0x0160–0x0168

5.3.1 EEE_CTRL

Address offset: 0x0100

Table 5-44 summarizes the EEE control register.

Table 5-44 EEE_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:14	RO	0	RESERVED	
13	R/W	0	RESERVED	
12	R/W	1	LPI_EN_5	LPI enable for port5
11	R/W	0	RESERVED	
10	R/W	1	LPI_EN_4	LPI enable for port4
9	R/W	0	RESERVED	
8	R/W	1	LPI_EN_3	LPI enable for port3
7	R/W	0	RESERVED	
6	R/W	1	LPI_EN_2	LPI enable for port2
5	R/W	0	RESERVED	
4	R/W	1	LPI_EN_1	LPI enable for port1 Enable PHY sleep
3	R/W	0	EEE_CPU_CHANGE_EN	1 = CPU can set the resolved value
2	R/W	0	EEE_LLDP_TO_CPU_EN	0 = EEE LLDP packet to deheader 1 = EEE LLDP packet to CPU
1	R/W	0	EEE_EN	1 = Support LLDP auto-negotiation PHY wake-up time
0	RO	0	RESERVED	

5.3.2 EEE_LOC_VALUE_1

Address offset: 0x0120

Table 5-45 summarizes the port 1 EEE variable register 0.

Table 5-45 EEE_LOC_VALUE1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	R/W	0	LOC_RX_VALUE_1	LocRxSystemValue
15:0	R/W	0	LOC_TX_VALUE_1	LocTxSystemValue

5.3.3 EEE_REM_VALUE_1

Address offset: 0x0124

Table 5-46 summarizes the port 1 EEE variable register 1.

Table 5-46 EEE_REM_VALUE_1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	R/W	0	ECHO_RX_VALUE_1	LocResolvedRxSystemValueEcho
15:0	R/W	0	ECHO_TX_VALUE_1	LocResolvedTxSystemValueEcho

5.3.4 EEE_RES_VALUE_1

Address offset: 0x0128

Table 5-47 summarizes the port 1 EEE variable register 2.

Table 5-47 EEE_RES_VALUE_1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	LOC_RESOLVED_RX_VALUE_1	LocResolvedRxSystemValueEcho
15:0	RO	0	LOC_RESOLVED_TX_VALUE_1	LocResolvedTxSystemValueEcho

5.3.5 EEE_LOC_VALUE_2

Address offset: 0x0130

Table 5-48 summarizes the port 2 EEE variable register 0.

Table 5-48 EEE_LOC_VALUE_2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	R/W	0	LOC_RX_VALUE_2	LocRxSystemValue
15:0	R/W	0	LOC_TX_VALUE_2	LocTxSystemValue

5.3.6 EEE_REM_VALUE_2

Address offset: 0x0134

Table 5-49 summarizes the port 2 EEE variable register 1.

Table 5-49 EEE_REM_VALUE_2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	R/W	0	ECHO_RX_VALUE_2	LocRxSystemValueEcho
15:0	R/W	0	ECHO_TX_VALUE_2	LocTxSystemValueEcho

5.3.7 EEE_RES_VALUE_2

Address offset: 0x0138

Table 5-50 summarizes the port 2 EEE variable register 2.

Table 5-50 EEE_RES_VALUE_2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	LOC_RESOLVED_RX_VALUE_2	LocResolvedRxSystemValueEcho
15:0	RO	0	LOC_RESOLVED_TX_VALUE_2	LocResolvedTxSystemValueEcho

5.3.8 EEE_LOC_VALUE_3

Address offset: 0x0140

Table 5-51 summarizes the port 3 EEE variable register 0.

Table 5-51 EEE_LOC_VALUE_3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	R/W	0	LOC_RX_VALUE_3	LocRxSystemValue
15:0	R/W	0	LOC_TX_VALUE_3	LocTxSystemValue

5.3.9 EEE_REM_VALUE_3

Address offset: 0x0144

Table 5-52 summarizes the port 3 EEE variable register 1.

Table 5-52 EEE_REM_VALUE_3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	R/W	0	ECHO_RX_VALUE_3	LocRxSystemValueEcho
15:0	R/W	0	ECHO_TX_VALUE_3	LocTxSystemValueEcho

5.3.10 EEE_RES_VALUE_3

Address offset: 0x0148

Table 5-53 summarizes the port 3 EEE variable register 2.

Table 5-53 EEE_RES_VALUE_3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	LOC_RESOLVED_RX_VALUE_3	LocResolvedRxSystemValueEcho
15:0	RO	0	LOC_RESOLVED_TX_VALUE_3	LocResolvedTxSystemValueEcho

5.3.11 EEE_LOC_VALUE_4

Address offset: 0x0150

Table 5-54 summarizes the port 4 EEE variable register 0.

Table 5-54 EEE_LOC_VALUE_4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	LOC_RX_VALUE_4	LocRxSystemValue
15:0	RO	0	LOC_TX_VALUE_4	LocTxSystemValue

5.3.12 EEE_REM_VALUE_4

Address offset: 0x0154

Table 5-55 summarizes the port 4 EEE variable register 1.

Table 5-55 EEE_REM_VALUE_4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	ECHO_RX_VALUE_4	LocRxSystemValueEcho
15:0	RO	0	ECHO_TX_VALUE_4	LocTxSystemValueEcho

5.3.13 EEE_RES_VALUE_4

Address offset: 0x0158

Table 5-56 summarizes the port 4 EEE variable register 2.

Table 5-56 EEE_RES_VALUE_4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	LOC_RESOLVED_RX_VALUE_4	LocResolvedRxSystemValueEcho
15:0	RO	0	LOC_RESOLVED_TX_VALUE_4	LocResolvedTxSystemValueEcho

5.3.14 EEE_LOC_VALUE_5

Address offset: 0x0160

Table 5-57 summarizes the port 5 EEE variable register 0.

Table 5-57 EEE_LOC_VALUE_5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	R/W	0	LOC_RX_VALUE_5	LocRxSystemValue
15:0	R/W	0	LOC_TX_VALUE_5	LocTxSystemValue

5.3.15 EEE_REM_VALUE_5

Address offset: 0x0164

Table 5-58 summarizes the port 5 EEE variable register 1.

Table 5-58 EEE_REM_VALUE_5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	R/W	0	ECHO_RX_VALUE_5	LocRxSystemValueEcho
15:0	R/W	0	ECHO_TX_VALUE_5	LocTxSystemValueEcho

5.3.16 EEE_RES_VALUE_5

Address offset: 0x0168

Table 5-59 summarizes the port 5 EEE variable register 2.

Table 5-59 EEE_RES_VALUE_5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	LOC_RESOLVED_RX_VALUE_5	LocResolvedRxSystemValueEcho
15:0	RO	0	LOC_RESOLVED_TX_VALUE_5	LocResolvedTxSystemValueEcho

5.4 Parser control registers (offset range: 0x0200–0x0270)

Table 5-60 summarizes the parser registers.

Table 5-60 Parser register summary

Name	Offset range
Normalize control register	0x0200–0x0204
Normalize length control register	0x0208
Frame acknowledge control register	0x0210–0x0214
Window rule control register	0x0218–0x024C
Trunk hash enable register	0x0270

5.4.1 NORMALIZE_CTRL0

Address offset: 0x0200

Table 5-61 summarizes the normalize control 0 register.

Table 5-61 NORMALIZE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29	R/W0	0	TCP_PSH1_ACK0_DROP_EN	1 = Frame with PUSH=1 & ACK=0 is dropped.
28	R/W0	0	TCP_FIN1_ACK0_DROP_EN	1 = Frame with FIN=1 & ACK=0 is dropped.
27	R/W0	0	TCP_RST1_WITH_DATA_DROP_EN	1 = Frame with RST=1 and IP_LEN - IP_HDR_LEN - TCP_OFFSET > 0 is dropped.
26	R/W	0	TCP_SYN1_WITH_DATA_DROP_EN	1 = Frame with SYN=1 and IP_LEN - IP_HDR_LEN - TCP_OFFSET > 0 is dropped.
25	R/W	0	TCP_RST1_DROP_EN	1 = Frame with RST=1 is dropped.

Table 5-61 NORMALIZE_CTRL0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
24	R/W	0	TCP_SYN0_ACK0_RST0_DROP_EN	1 = Frame with SYN=0 & ACK=0 & RST=0 is dropped.
23	R/W	0	TCP_SYN1_FIN1_DROP_EN	1 = Frame with SYN=1 & FIN=1 is dropped.
22	R/W	0	TCP_SYN1_RST1_DROP_EN	1 = Frame with SYN=1 & RST=1 is dropped.
21	R/W	0	TCP_NULLSCAN_DROP_EN	1 = Frame with Seq_Num=0 and all TCP FLAG zero is dropped.
20	R/W	0	TCP_XMASSCAN_DROP_EN	1 = Frame with Seq_Num=0, FIN=1, URG=1, and PSH=1 is dropped
19	RO	0	TCP_SYN1_ACK1_PSH1_DROP_EN	1 = Frame with SYN=1 & ACK=1 & PSH=1 is dropped.
18	RO	0	TCP_SYN1_PSH1_DROP_EN	1 = Frame with SYN=1 & PSH=1 is dropped.
17	RO	0	TCP_SYN1_URG1_DROP_EN	1 = Frame with SYN=1 & URG=1 is dropped.
16	RO	0	TCP_SYN_ERR_DROP_EN	1 = Frame with SYN=1 & ACK=0 & SP<1024 is dropped
15	RO	0	TCP_HDR_MIN_DROP_EN	1 = If frame with TCP header length less than TCP_HDR_MIN_SIZE, but not first of fragment, is dropped
14	R/W	0	TCP_SAME_PORT_DROP_EN	1 = TCP frame with SP equal to DP is dropped.
13	R/W	0	IPV4_CHECKSUM_DROP_EN	1 = Frame with IPv4 checksum error is dropped.
12	R/W	0	IPV4_DIP_ERR_DROP_EN	1 = Frame is dropped if with DIP all zero, or DIP[31:24] is 0x7F.
11	R/W	0	IPV4_SIP_ERR_DROP_EN	1 = Frame is dropped if with SIP[31:24] more than 0xE0 and less than 0xF0, or equal to 0x7F, or SIP[31:0] is 0x32'hFFFFFFFF.
10	R/W	0	IPV4_FRAG_LEN_DROP_EN	1 = Frame with IPv4 fragment length check error is dropped.
9	R/W	0	IPV4_FRAG_MAX_DROP_EN	
8	R/W	0	IPV4_FRAG_MIN_DROP_EN	1 = Frame with offset length less than minimum is dropped
7	R/W	0	IPV4_DF_DROP_EN	1 = Frame with DF=1 and offset or MF not zero, is dropped
6	R/W	0	IP_LEN_DROP_EN	1 = Frame with IP length field error is dropped, IPv4 and IPv6 included.
5	R/W	0	IPV4_HDR_LEN_CHECK_EN	1 = Check the IP options. If frame is with options, drop or send to CPU
4	R/W	0	IPV4_HDR_LEN_DROP_EN	This bit can be used to forward or drop frame when IPv4 header length check fail.
3	RO	0	IPV4_HDR_LEN_MIN_DROP_EN	0 = Frame with IPv4 header length check error is sent to CPU port (only to CPU port)

Table 5-61 NORMALIZE_CTRL0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
2	R/W	0	IP_SAME_PORT_DROP_EN	1 = Frame with IPv4 header length check error is dropped.
1	R/W	0	IP_VER_DROP_EN	1 = Frame is dropped if IPv4 header length less than 20 byte.
0	R/W	0	VID_4095_DROP_EN	1 = Frame is drop if SIP equal to DIP.

5.4.2 NORMALIZE_CTRL1

Address offset: 0x0204

Table 5-62 summarizes the normalize control 1 register.

Table 5-62 NORMALIZE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	R/W	0	IPV4_FRAG_MIN	Define the minimum length of IPv4 frame with fragment
23:21	R/O	0	RESERVED	
20	R/W	0	INVALID_MAC_SRC_ADDR_DROP_EN	SA is broadcast or multicast address. The frame is dropped by the switch.
19	R/W	0	IPV4_MIN_PKT_LEN_DROP_EN	If the frame length is less than the minimum IPv4 frame size.
18	R/W	0	IPV6_MIN_PKT_LEN_DROP_EN	If the frame length is less than the minimum IPv6 frame size
17	R/W	0	INVALID_SIP6_DROP_EN	Drop Invalid Source IP for IPv6 IP is ::1 or ff00::/8
16	R/W	0	INVALID_DIP6_DROP_EN	Drop Invalid Destination IP for IPv6 \ IP is ::1 or ::/128
15:12	R/W	0	TCP_HDR_MIN_SIZE	Defined the minimum size of TCP header
11	R/W	0	ICMP_CHECKSUM_DROP_EN	Drop the ICMP checksum error
10	R/W	0	ICMPV6_FRAG_DROP_EN	1 = Frame with fragment ICMPv6 is dropped.
9	R/W	0	ICMPV4_FRAG_DROP_EN	1 = Frame with fragment ICMPv4 is dropped.
8	R/W	0	ICMPV6_MAX_LEN_DROP_EN	1 = Frame with un-fragment ICMPv6 length larger than ICMPV6_MAX_LEN is dropped.
7	R/W	0	ICMPV4_MAX_LEN_DROP_EN	1 = Frame with un-fragment ICMPv4 length larger than ICMPV4_MAX_LEN is dropped.
6	R/W	0	UDP_CHECKSUM_DROP_EN	1 = Frame with UDP checksum error is dropped.

Table 5-62 NORMALIZE_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
5	R/W	0	UDP_LEN_DROP_EN	1 = Frame with UDP length check error is dropped.
4	R/W	0	UDP_SAME_PORT_DROP_EN	1 = UDP frame with SP equal to DP is dropped.
3	R/W	0	TCP_OPTION_DROP_EN	1 = Frame with SYN=0 and IP header larger than 20 byte, is dropped.
2	R/W	0	TCP_URG0_PTR_ERR_DROP_EN	1 = Frame with URG=0 but pointer not zero is dropped.
1	R/W	0	TCP_CHECKSUM_DROP_EN	1 = Frame with TCP checksum error is dropped.
0	R/W	0	TCP_URG1_ACK0_DROP_EN	1 = Frame with URG=1 & ACK=0 is dropped.

5.4.3 NORMALIZE_LEN_CTRL

Address offset: 0x0208

Table 5-63 summarizes the normalize length control register.

Table 5-63 NORMALIZE_LEN_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29:16	R/W	0x40	ICMPV6_MAX_LEN	Defined the maximum IP payload length of ICMPv6 frame
15:14	RO	0	RESERVED	
13:0	R/W	0x40	ICMPV4_MAX_LEN	Defined the maximum IP payload length of ICMPv4 frame

5.4.4 FRAM_ACK_CTRL0

Address offset: 0x00210

Table 5-64 summarizes the frame ACK control 0 register.

Table 5-64 FRAM_ACK_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30	R/W	0	ARP_REQ_EN_3	See bit[6]
29	R/W	0	ARP_ACK_EN_3	See bit[5]
28	R/W	0	DHCP_EN_3	See bit[4]

Table 5-64 FRAM_ACK_CTRL0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
27	R/W	0	EAPOL_EN_3	See bit[3]
26	R/W	0	IGMP_LEAVE_EN_3	See bit[2]
25	R/W	0	IGMP_JOIN_EN_3	See bit[1]
24	R/W	0	IGMP_MLD_EN_3	See bit[0]
23	RO	0	RESERVED	
22	R/W	0	ARP_REQ_EN_2	See bit[6]
21	R/W	0	ARP_ACK_EN_2	See bit[5]
20	R/W	0	DHCP_EN_2	See bit[4]
19	R/W	0	EAPOL_EN_2	See bit[3]
18	R/W	0	IGMP_LEAVE_EN_2	See bit[2]
17	R/W	0	IGMP_JOIN_EN_2	See bit[1]
16	R/W	0	IGMP_MLD_EN_2	See bit[0]
15	RO	0	RESERVED	
14	R/W	0	ARP_REQ_EN_1	See bit[6]
13	R/W	0	ARP_ACK_EN_1	See bit[5]
12	R/W	0	DHCP_EN_1	See bit[4]
11	R/W	0	EAPOL_EN_1	See bit[3]
10	R/W	0	IGMP_LEAVE_EN_1	See bit[2]
9	R/W	0	IGMP_JOIN_EN_1	See bit[1]
8	R/W	0	IGMP_MLD_EN_1	See bit[0]
7	RO	0	RESERVED	
6	R/W	0	ARP_REQ_EN_0	ARP request frame acknowledge enable
5	R/W	0	ARP_ACK_EN_0	ARP response frame acknowledge enable
4	R/W	0	DHCP_EN_0	0 = Acknowledge DHCP frame disable 1 = Acknowledge DHCP frame enable
3	R/W	0	EAPOL_EN_0	1 = Hardware acknowledge 802.1x frame, and send frame copy or redirect to CPU controlled by EAPAL_REDIRRECT_EN
2	R/W	0	IGMP_LEAVE_EN_0	1 = Enable IGMP/MLD hardware fast leave
1	R/W	0	IGMP_JOIN_EN_0	1 = Enable IGMP/MLD hardware join
0	R/W	0	IGMP_MLD_EN_0	IGMP/MLD snooping enable. If this bit is set to 1, the port examines all received frames and copy or redirect to CPU port controlled by IGMP_COPY_EN.

5.4.5 FRAM_ACK_CTRL1

Address offset: 0x00214

Table 5-65 summarizes the frame ACK control 1 register.

Table 5-65 FRAM_ACK_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:26	RO	0	RESERVED	
25	R/W	0	PPPOE_EN	0 = PPPoE package acknowledge disable 1 = PPPoE package acknowledge enable
24	R/W	0	IGMP_V3_EN	0 = IGMPv3 or MLDv2 acknowledge disable 1 = IGMPv3 or MLDv2 acknowledge enable
23	RO	0	RESERVED	
22	R/W	0	ARP_REQ_EN_6	See bit[6]
21	R/W	0	ARP_ACK_EN_6	See bit[5]
20	R/W	0	DHCP_EN_6	See bit[4]
19	R/W	0	EAPOL_EN_6	See bit[3]
18	R/W	0	IGMP_LEAVE_EN_6	See bit[2]
17	R/W	0	IGMP_JOIN_EN_6	See bit[1]
16	R/W	0	IGMP_MLD_EN_6	See bit[0]
15	RO	0	RESERVED	
14	R/W	0	ARP_REQ_EN_5	See bit[6]
13	R/W	0	ARP_ACK_EN_5	See bit[5]
12	R/W	0	DHCP_EN_5	See bit[4]
11	R/W	0	EAPOL_EN_5	See bit[3]
10	R/W	0	IGMP_LEAVE_EN_5	See bit[2]
9	R/W	0	IGMP_JOIN_EN_5	See bit[1]
8	R/W	0	IGMP_MLD_EN_5	See bit[0]
7	RO	0	RESERVED	
6	R/W	0	ARP_REQ_EN_4	ARP request frame acknowledge enable
5	R/W	0	ARP_ACK_EN_4	ARP response frame acknowledge enable
4	R/W	0	DHCP_EN_4	0 = Acknowledge DHCP frame disable 1 = Acknowledge DHCP frame enable
3	R/W	0	EAPOL_EN_4	1 = Hardware acknowledge 802.1x frame, and send frame copy or redirect to CPU controlled by EAPAL_REDIRECT_EN.
2	R/W	0	IGMP_LEAVE_EN_4	1 = Enable IGMP/MLD hardware fast leave
1	R/W	0	IGMP_JOIN_EN_4	1 = Enable IGMP/MLD hardware join
0	R/W	0	IGMP_MLD_EN_4	IGMP/MLD snooping enable. If this bit is set to 1, the port examines all received frames and copies or redirects to CPU port controlled by IGMP_COPY_EN.

5.4.6 WIN_RULE_CTRL0

Address offset: 0x0218

Table 5-66 summarizes the window rule control 0 register.

Table 5-66 WIN_RULE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	RO	0	RESERVED	
27:24	R/W	0	L4_LENGTH_0	These bits indicate that window rule in port0 to select length of L4, from L4_OFFSET_0.
23:20	R/W	0	L3_LENGTH_0	These bits indicate that window rule in port0 to select length of L3, from L3_OFFSET_0.
19:16	R/W	0	L2_LENGTH_0	These bits indicate that window rule in port0 to select length of L2, from L2_OFFSET_0.
15	RO	0	RESERVED	
14:10	R/W	0	L4_OFFSET_0	These bits indicate that window rule in port0 to select offset of L3, from TCP/UDP header.
9:5	R/W	0	L3_OFFSET_0	These bits indicate that window rule in port0 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_0	These bits indicate that window rule in port0 to select offset of L2, from MAC DA.

5.4.7 WIN_RULE_CTRL1

Address offset: 0x021C

Table 5-67 summarizes the window rule control 1 register.

Table 5-67 WIN_RULE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	RO	0	RESERVED	
27:24	R/W	0	L4_LENGTH_1	These bits indicate that window rule in port1 to select length of L4, from L4_OFFSET_1.
23:20	R/W	0	L3_LENGTH_1	These bits indicate that window rule in port1 to select length of L3, from L3_OFFSET_1.
19:16	R/W	0	L2_LENGTH_1	These bits indicate that window rule in port1 to select length of L2, from L2_OFFSET_1.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_1	These bits indicate that window rule in port1 to select offset of L3, from TCP/UDP header.

Table 5-67 WIN_RULE_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
9:5	R/W	0	L3_OFFSET_1	These bits indicate that window rule in port1 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_1	These bits indicate that window rule in port1 to select offset of L2, from MAC DA.

5.4.8 WIN_RULE_CTRL2

Address offset: 0x0220

Table 5-68 summarizes the window rule control 2 register.

Table 5-68 WIN_RULE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	RO	0	RESERVED	
27:24	R/W	0	L4_LENGTH_2	These bits indicate that window rule in port2 to select length of L4, from L4_OFFSET_2.
23:20	R/W	0	L3_LENGTH_2	These bits indicate that window rule in port2 to select length of L3, from L3_OFFSET_2.
19:16	R/W	0	L2_LENGTH_2	These bits indicate that window rule in port2 to select length of L2, from L2_OFFSET_2.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_2	These bits indicate that window rule in port2 to select offset of L3, from TCP/UDP header.
9:5	R/W	0	L3_OFFSET_2	These bits indicate that window rule in port2 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_2	These bits indicate that window rule in port2 to select offset of L2, from MAC DA.

5.4.9 WIN_RULE_CTRL3

Address offset: 0x0224

Table 5-69 summarizes the window rule control 3 register.

Table 5-69 WIN_RULE_CTRL3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	RO	0	RESERVED	
27:24	R/W	0	L4_LENGTH_3	These bits indicate that window rule in port3 to select length of L4, from L4_OFFSET_3.

Table 5-69 WIN_RULE_CTRL3 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
23:20	R/W	0	L3_LENGTH_3	These bits indicate that window rule in port3 to select length of L3, from L3_OFFSET_3.
19:16	R/W	0	L2_LENGTH_3	These bits indicate that window rule in port3 to select length of L2, from L2_OFFSET_3.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_3	These bits indicate that window rule in port3 to select offset of L3, from TCP/UDP header.
9:5	R/W	0	L3_OFFSET_3	These bits indicate that window rule in port3 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_3	These bits indicate that window rule in port3 to select offset of L2, from MAC DA.

5.4.10 WIN_RULE_CTRL4

Address offset: 0x0228

Table 5-70 summarizes the window rule control 4 register.

Table 5-70 WIN_RULE_CTRL4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	RO	0	RESERVED	
27:24	R/W	0	L4_LENGTH_4	These bits indicate that window rule in port4 to select length of L4, from L4_OFFSET_4.
23:20	R/W	0	L3_LENGTH_4	These bits indicate that window rule in port4 to select length of L3, from L3_OFFSET_4.
19:16	R/W	0	L2_LENGTH_4	These bits indicate that window rule in port4 to select length of L2, from L2_OFFSET_4.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_4	These bits indicate that window rule in port4 to select offset of L3, from TCP/UDP header.
9:5	R/W	0	L3_OFFSET_4	These bits indicate that window rule in port4 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_4	These bits indicate that window rule in port4 to select offset of L2, from MAC DA.

5.4.11 WIN_RULE_CTRL5

Address offset: 0x022C

Table 5-71 summarizes the window rule control 5 register.

Table 5-71 WIN_RULE_CTRL5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	RO	0	RESERVED	
27:24	R/W	0	L4_LENGTH_5	These bits indicate that window rule in port5 to select length of L4, from L4_OFFSET_5.
23:20	R/W	0	L3_LENGTH_5	These bits indicate that window rule in port5 to select length of L3, from L3_OFFSET_5.
19:16	R/W	0	L2_LENGTH_5	These bits indicate that window rule in port5 to select length of L2, from L2_OFFSET_5.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_5	These bits indicate that window rule in port5 to select offset of L3, from TCP/UDP header.
9:5	R/W	0	L3_OFFSET_5	These bits indicate that window rule in port5 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_5	These bits indicate that window rule in port5 to select offset of L2, from MAC DA.

5.4.12 WIN_RULE_CTRL6

Address offset: 0x0230

Table 5-72 summarizes the window rule control 6 register.

Table 5-72 WIN_RULE_CTRL6 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	RO	0	RESERVED	
27:24	R/W	0	L4_LENGTH_6	These bits indicate that window rule in port6 to select length of L4, from L4_OFFSET_6.
23:20	R/W	0	L3_LENGTH_6	These bits indicate that window rule in port6 to select length of L3, from L3_OFFSET_6.
19:16	R/W	0	L2_LENGTH_6	These bits indicate that window rule in port6 to select length of L2, from L2_OFFSET_6.
15	R/W	0	RESERVED	
14:10	R/W	0	L4_OFFSET_6	These bits indicate that window rule in port6 to select offset of L3, from TCP/UDP header.
9:5	R/W	0	L3_OFFSET_6	These bits indicate that window rule in port6 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET_6	These bits indicate that window rule in port6 to select offset of L2, from MAC DA.

5.4.13 WIN_RULE_CTRL7

Address offset: 0x0234

Table 5-73 summarizes the window rule control 7 register.

Table 5-73 WIN_RULE_CTRL7 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_0	These bits indicate that window rule in port0 to select length of L3, from L3_OFFSET1_0.
19:16	R/W	0	L2_LENGTH1_0	These bits indicate that window rule in port0 to select length of L2, from L2_OFFSET1_0.
15:10	R/W	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_0	These bits indicate that window rule in port0 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET1_0	These bits indicate that window rule in port0 to select offset of L2, from the end of snap.

5.4.14 WIN_RULE_CTRL8

Address offset: 0x0238

Table 5-74 summarizes the window rule control 8 register.

Table 5-74 WIN_RULE_CTRL8 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_1	These bits indicate that window rule in port1 to select length of L3, from L3_OFFSET1_0.
19:16	R/W	0	L2_LENGTH1_1	These bits indicate that window rule in port1 to select length of L2, from L2_OFFSET1_0.
15:10	RO	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_1	These bits indicate that window rule in port1 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET1_1	These bits indicate that window rule in port1 to select offset of L2, from the end of snap.
4:0	RO	0	RESERVED	

5.4.15 WIN_RULE_CTRL9

Address offset: 0x023C

Table 5-75 summarizes the window rule control 9 register.

Table 5-75 WIN_RULE_CTRL9 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_2	These bits indicate that window rule in port2 to select length of L3, from L3_OFFSET1_0.
19:16	R/W	0	L2_LENGTH1_2	These bits indicate that window rule in port2 to select length of L2, from L2_OFFSET1_0.
15:10	RO	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_2	These bits indicate that window rule in port2 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET1_2	These bits indicate that window rule in port2 to select offset of L2, from the end of snap.

5.4.16 WIN_RULE_CTRL10

Address offset: 0x0240

Table 5-76 summarizes the window rule control 10 register.

Table 5-76 WIN_RULE_CTRL10 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_3	These bits indicate that window rule in port3 to select length of L3, from L3_OFFSET1_0.
19:16	R/W	0	L2_LENGTH1_3	These bits indicate that window rule in port3 to select length of L2, from L2_OFFSET1_0.
15:10	R/W	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_3	These bits indicate that window rule in port3 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET1_3	These bits indicate that window rule in port3 to select offset of L2, from the end of snap.

5.4.17 WIN_RULE_CTRL11

Address offset: 0x0244

Table 5-77 summarizes the window rule control 11 register.

Table 5-77 WIN_RULE_CTRL11 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_4	These bits indicate that window rule in port4 to select length of L3, from L3_OFFSET1_0.
19:16	R/W	0	L2_LENGTH1_4	These bits indicate that window rule in port4 to select length of L2, from L2_OFFSET1_0.
15:10	R/W	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_4	These bits indicate that window rule in port4 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET1_4	These bits indicate that window rule in port4 to select offset of L2, from the end of snap.

5.4.18 WIN_RULE_CTRL12

Address offset: 0x0248

Table 5-78 summarizes the window rule control 12 register.

Table 5-78 WIN_RULE_CTRL12 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_5	These bits indicate that window rule in port5 to select length of L3, from L3_OFFSET1_0.
19:16	R/W	0	L2_LENGTH1_5	These bits indicate that window rule in port5 to select length of L2, from L2_OFFSET1_0.
15:10	R/W	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_5	These bits indicate that window rule in port5 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET1_5	These bits indicate that window rule in port5 to select offset of L2, from the end of snap.

5.4.19 WIN_RULE_CTRL13

Address offset: 0x024C

Table 5-79 summarizes the window rule control 13 register.

Table 5-79 WIN_RULE_CTRL13 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:20	R/W	0	L3_LENGTH1_6	These bits indicate that window rule in port6 to select length of L3, from L3_OFFSET1_0.
19:16	R/W	0	L2_LENGTH1_6	These bits indicate that window rule in port6 to select length of L2, from L2_OFFSET1_0.
15:10	R/W	0	RESERVED	
9:5	R/W	0	L3_OFFSET1_6	These bits indicate that window rule in port6 to select offset of L3, from IP header.
4:0	R/W	0	L2_OFFSET1_6	These bits indicate that window rule in port6 to select offset of L2, from the end of snap.

5.4.20 TRUNK_HASH_EN

Address offset: 0x0270

Table 5-80 summarizes the trunk hash enable register.

Table 5-80 TRUNK_HASH_EN bit description

Bits	R/W	Initial value	Mnemonic	Description
31:4	RO	0	RESERVED	
3	R/W	0	TRUNK_HASH_SIP_EN	SIP join the trunk hash
2	R/W	0	TRUNK_HASH_DIP_EN	DIP join the trunk hash
1	R/W	0	TRUNK_HASH_SA_EN	SA join the trunk hash
0	R/W	0	TRUNK_HASH_DA_EN	DA join the trunk hash

5.5 ACL register (offset range: 0x0400–0x0454)

Table 5-81 summarizes the ACL registers.

Table 5-81 ACL register summary

Name	Offset range
ACL function register	0x0400–0x0414
VLAN translation test register	0x0418
Port0 VLAN control register	0x0420–0x0424
Port1 VLAN control register	0x0428–0x042C
Port2 VLAN control register	0x0430–0x0434
Port3 VLAN control register	0x0438–0x043C

Table 5-81 ACL register summary (cont.)

Name	Offset range
Port4 VLAN control register	0x0440–0x0444
Port5 VLAN control register	0x0448–0x044C
Port6 VLAN control register	0x0450–0x0454

5.5.1 ACL_FUNC0

Address offset: 0x0400

Table 5-82 summarizes the ACL function 0 register.

Table 5-82 ACL_FUNC0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	ACL_BUSY	Depend: ACL_DONE_INT, ACL table busy. This bit must be set to 1 to start a ACL operation and cleared to 0 after operation done. If this bit is set to 1, CPU can not request another operation.
30:11	RO	0	RESERVED	
10	R/W	0	ACL_FUNC	0 = Write 1 = Read
9:8	R/W	0	ACL_RULE_SEL	ACL rule selection: 00 = Rule 01 = Mask 10 = Result 11 = Reserved
7	RO	0	RESERVED	
6:0	R/W	0	ACL_FUNC_INDEX	ACL rule index

5.5.2 ACL_FUNC1

Address offset: 0x0404

Table 5-83 summarizes the ACL function 1 register.

Table 5-83 ACL_FUNC1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ACL_RULE_DATA_0	ACL rule: byte[3:0]

5.5.3 ACL_FUNC2

Address offset: 0x0408

Table 5-84 summarizes the ACL function 2 register.

Table 5-84 ACL_FUNC2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ACL_RULE_DATA_1	ACL rule: byte[7:4]

5.5.4 ACL_FUNC3

Address offset: 0x040C

Table 5-85 summarizes the ACL function 3 register.

Table 5-85 ACL_FUNC3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ACL_RULE_DATA_2	ACL rule: byte[11:8]

5.5.5 ACL_FUNC4

Address offset: 0x0410

Table 5-86 summarizes the ACL function 4 register.

Table 5-86 ACL_FUNC4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ACL_RULE_DATA_3	ACL rule: byte[15:12]

5.5.6 ACL_FUNC5

Address offset: 0x0414

Table 5-87 summarizes the ACL function 5 register.

Table 5-87 ACL_FUNC5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:8	R/W	0	RESERVED	
7:0	R/WW	0	ACL_RULE_DATA_4	ACL rule: byte[16]

5.5.7 VLAN_TRANS_TEST

Address offset: 0x0418

Table 5-88 summarizes the VLAN translation test register.

Table 5-88 VLAN_TRANS_TEST bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	VLAN_TRANS_TEST_EN	
30:2	RO	0	RESERVED	
1	R/W	0	EG_TRANS_FLTR_BYPASS_EN	Translation filter bypass enable Only valid for not 1:1 entry when doing second QinQ lookup. If it's valid, the forwarding member is set to 0x7f.
0	R/W	0	NET_ISOLATE_EN	1 = Isolate private net and public net. The packet is dropped at layer forwarding when DIP is private IP but SIP is not private IP.

5.5.8 PORT0_VLAN_CTRL0

Address offset: 0x0420

Table 5-89 summarizes the port 0 VLAN control 0 register.

Table 5-89 PORT0_VLAN_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_0	Port default CVLAN priority for received frames.
28	RO	0	RESERVED	
27:16	R/W	0x1	PORT_DEFAULT_CVID_0	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_0	Port default SVLAN priority for received frames.
12	RO	0	RESERVED	
11:0	R/W	0x1	PORT_DEFAULT_SVID_0	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.

5.5.9 PORT0_VLAN_CTRL1

Address offset: 0x0424

Table 5-90 summarizes the port 0 VLAN control 1 register.

Table 5-90 PORT0_VLAN_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:15	RO	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_0	0 = All frames can be sent out. 1 = Only tagged frames can be sent out.
13:12	R/W	11	EG_VLAN_MODE_0	Egress VLAN mode 00 = Egress transmits frames unmodified 01 = Egress transmits frames without VLAN 10 = Egress transmits frames with VLAN 11 = Untouched
11	RO	0	RESERVED	
10	RO	0	SPCHECK_EN_0	1 = L3 source port check enable
9	R/W	0	CORE_PORT_EN_0	0 = Edge port 1 = Core port
8	R/W	0	FORCE_DEFAULT_VID_EN_0	0 = Use frame tag only. 1 = Force to use port default VID and priority for received frame, when 802.1q mode is not disable.
7	R/W	0	PORT_TLS_MODE_0	0 = Port work at NON-TLS mode 1 = Port work at TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_0	1 = Enable part-based VLAN propagate function.
5	R/W	0	PORT_CLONE_EN_0	0 = Enable port replace 1 = Enable port clone
4	R/W	0	VLAN_PRI_PRO_EN_0	1 = VLAN priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_0	00 = All frame can be received by this port, including untagged and tagged frames. 01 = Only frame with tag can be received by this port. 10 = Only frame untagged can be received by this port, including no VLAN and priority VLAN. 11 = Reserved
1:0	RO	0	RESERVED	

5.5.10 PORT1_VLAN_CTRL0

Address offset: 0x0428

Table 5-91 summarizes the port 1 VLAN control 0 register.

Table 5-91 PORT1_VLAN_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_1	Port default CVLAN priority for received frames.
28	RO	0	RESERVED	
27:16	R/W	0X1	PORT_DEFAULT_CVID_1	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_1	Port default SVLAN priority for received frames.
12	RO	0	RESERVED	
11:0	R/W	0X1	PORT_DEFAULT_SVID_1	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.

5.5.11 PORT1_VLAN_CTRL1

Address offset: 0x042C

Table 5-92 summarizes the port 1 VLAN control 1 register.

Table 5-92 PORT1_VLAN_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:15	RO	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_1	0 = All frames can be sent out. 1 = Only tagged frames can be sent out.
13:12	R/W	3	EG_VLAN_MODE_1	Egress VLAN mode. 00 = Egress transmits frames unmodified. 01 = Egress transmits frames without VLAN 10 = Egress transmits frames with VLAN 11 = Untouched
11	RO	0	RESERVED	
10	R/W	0	SPCHECK_EN_1	1 = L3 Source port check enable
9	R/W	0	CORE_PORT_EN_1	0 = Edge port 1 = Core port
8	R/W	0	FORCE_DEFAULT_VID_EN_1	0 = Use frame tag only. 1 = Force to use port default VID and priority for received frame, when 802.1q mode is not disable.
7	R/W	0	PORT_TLS_MODE_1	0 = Port work at NON-TLS mode 1 = Port work at TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_1	1 = Enable part-based VLAN propagate function.

Table 5-92 PORT1_VLAN_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
5	R/W	0	PORT_CLONE_EN_1	0 = Enable port replace 1 = Enable port clone
4	R/W	0	VLAN_PRI_PRO_EN_1	1 = VLAN priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_1	00 = All Frame can be received by this port, including untagged and tagged frames. 01 = Only frame with tag can be received by this port. 10 = Only frame untagged can be received by this port, including no VLAN and priority VLAN. 11 = Reserved
0	RO	0	RESERVED	

5.5.12 PORT2_VLAN_CTRL0

Address offset: 0x0430

Table 5-93 summarizes the port 2 VLAN control 0 register.

Table 5-93 PORT2_VLAN_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_2	Port default CVLAN priority for received frames.
28	RO	0	RESERVED	
27:16	R/W	0x1	PORT_DEFAULT_CVID_2	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_2	Port default SVLAN priority for received frames.
12	RO	0	RESERVED	
11:0	R/W	0x1	PORT_DEFAULT_SVID_2	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.

5.5.13 PORT2_VLAN_CTRL1

Address offset: 0x0434

Table 5-94 summarizes the port 2 VLAN control 1 register.

Table 5-94 PORT2_VLAN_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:15	RO	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_2	0 = All frames can be sent out. 1 = Only tagged frames can be sent out.
13:12	R/W	3	EG_VLAN_MODE_2	Egress VLAN mode. 00 = Egress transmits frames unmodified 01 = Egress transmits frames without VLAN 10 = Egress transmits frames with VLAN 11 =Untouched
11	RO	0	RESERVED	
10	R/W	0	SPCHECK_EN_2	1 = L3 source port check enable
9	R/W	0	CORE_PORT_EN_2	0 = Edge port 1 = Core port
8	R/W	0	FORCE_DEFAULT_VID_EN_2	0 = Use frame tag only. 1 = Force to use port default VID and priority for received frame, when 802.1q mode is not disable.
7	R/W	0	PORT_TLS_MODE_2	0 = Port work at NON-TLS mode 1 = Port work at TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_2	1 = Enable part-based VLAN propagate function.
5	R/W	0	PORT_CLONE_EN_2	0 = Enable port replace 1 = Enable port clone
4	R/W	0	VLAN_PRI_PRO_EN_2	1 = VLAN priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_2	00 = All frame can be received by this port, including untagged and tagged frames. 01 = Only frame with tag can be received by this port. 10 = Only frame untagged can be received by this port, including no VLAN and priority VLAN. 11 = Reserved
0	RO	0	RESERVED	

5.5.14 PORT3_VLAN_CTRL0

Address offset: 0x0438

Table 5-95 summarizes the port 3 VLAN control 0 register.

Table 5-95 PORT3_VLAN_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_3	Port default CVLAN priority for received frames.
28	RO	0	RESERVED	
27:16	R/W	0X1	PORT_DEFAULT_CVID_3	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_3	Port default SVLAN priority for received frames.
12	RO	0	RESERVED	
11:0	R/W	0X1	PORT_DEFAULT_SVID_3	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.

5.5.15 PORT3_VLAN_CTRL1

Address offset: 0x043C

Table 5-96 summarizes the port 3 VLAN control 1 register.

Table 5-96 PORT3_VLAN_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:15	RO	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_3	0 = All frames can be sent out. 1 = Only tagged frames can be sent out.
13:12	R/W	3	EG_VLAN_MODE_3	Egress VLAN mode. 00 = Egress transmits frames unmodified 01 = Egress transmits frames without VLAN 10 = Egress transmits frames with VLAN 11 = Untouched
11	RO	0	RESERVED	
10	R/W	0	SPCHECK_EN_3	1 = L3 Source port check enable
9	R/W	0	CORE_PORT_EN_3	0 = Edge port 1 = Core port
8	R/W	0	FORCE_DEFAULT_VID_EN_3	0 = Use frame tag only. 1 = Force to use port default VID and priority for received frame, when 802.1q mode is not disable.
7	R/W	0	PORT_TLS_MODE_3	0 = Port work at NON-TLS mode 1 = Port work at TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_3	1 = Enable part-based VLAN propagate function.

Table 5-96 PORT3_VLAN_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
5	R/W	0	PORT_CLONE_EN_3	0 = Enable port replace 1 = Enable port clone
4	R/W	0	VLAN_PRI_PRO_EN_3	1 = VLAN priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_3	00 = All Frame can be received by this port, including untagged and tagged frames. 01 = Only frame with tag can be received by this port. 10 = Only frame untagged can be received by this port, including no VLAN and priority VLAN. 11 = Reserved
0	RO	0	RESERVED	

5.5.16 PORT4_VLAN_CTRL0

Address offset: 0x0440

Table 5-97 summarizes the port 4 VLAN control 0 register.

Table 5-97 PORT4_VLAN_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_4	Port default CVLAN priority for received frames.
28	RO	0	RESERVED	
27:16	R/W	0X1	PORT_DEFAULT_CVID_4	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_4	Port default SVLAN priority for received frames.
12	RO	0	RESERVED	
11:0	R/W	0X1	PORT_DEFAULT_SVID_4	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.

5.5.17 PORT4_VLAN_CTRL1

Address offset: 0x0444

Table 5-98 summarizes the port 4 VLAN control 1 register.

Table 5-98 PORT4_VLAN_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:15	RO	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_4	0 = All frames can be sent out. 1 = Only tagged frames can be sent out.
13:12	R/W	3	EG_VLAN_MODE_4	Egress VLAN mode. 00 = Egress transmits frames unmodified 01 = Egress transmits frames without VLAN 10 = Egress transmits frames with VLAN 11 = Untouched
11	RO	0	RESERVED	
10	R/W	0	SPCHECK_EN_4	1 = L3 Source port check enable
9	R/W	0	CORE_PORT_EN_4	0 = Edge port 1 = Core port
8	R/W	0	FORCE_DEFAULT_VID_EN_4	0 = Use frame tag only. 1 = Force to use port default VID and priority for received frame, when 802.1q mode is not disable.
7	R/W	0	PORT_TLS_MODE_4	0 = Port work at NON-TLS mode 1 = Port work at TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_4	1 = Enable part-based VLAN propagate function.
5	R/W	0	PORT_CLONE_EN_4	0 = Enable port replace 1 = Enable port clone
4	R/W	0	VLAN_PRI_PRO_EN_4	1 = VLAN priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_4	00 = All frame can be received by this port, including untagged and tagged frames. 01 = Only frame with tag can be received by this port. 10 = Only frame untagged can be received by this port, including no VLAN and priority VLAN. 11 = Reserved
0	RO	0	RESERVED	

5.5.18 PORT5_VLAN_CTRL0

Address offset: 0x0448

Table 5-99 summarizes the port 5 VLAN control 0 register.

Table 5-99 PORT5_VLAN_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_5	Port default CVLAN priority for received frames.
28	RO	0	RESERVED	
27:16	R/W	0X1	PORT_DEFAULT_CVID_5	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_5	Port default SVLAN priority for received frames.
12	RO	0	RESERVED	
11:0	R/W	0X1	PORT_DEFAULT_SVID_5	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.

5.5.19 PORT5_VLAN_CTRL1

Address offset: 0x044C

Table 5-100 summarizes the port 5 VLAN control 1 register.

Table 5-100 PORT5_VLAN_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:15	RO	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_5	0 = All Frames can be sent out. 1 = Only tagged frames can be sent out.
13:12	R/W	3	EG_VLAN_MODE_5	Egress VLAN mode. 00 = Egress transmits frames unmodified 01 = Egress transmits frames without VLAN 10 = Egress transmits frames with VLAN 11 = Untouched
11	RO	0	RESERVED	
10	R/W	0	SPCHECK_EN_5	1 = L3 Source port check enable
9	R/W	0	CORE_PORT_EN_5	0 = Edge port 1 = Core port
8	R/W	0	FORCE_DEFAULT_VID_EN_5	0 = Use frame tag only. 1 = Force to use port default VID and priority for received frame, when 802.1q mode is not disable.
7	R/W	0	PORT_TLS_MODE_5	0 = Port work at NON-TLS mode 1 = Port work at TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_5	1 = Enable part-based VLAN propagate function.

Table 5-100 PORT5_VLAN_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
5	R/W	0	PORT_CLONE_EN_5	0 = Enable port replace 1 = Enable port clone
4	R/W	0	VLAN_PRI_PRO_EN_5	1 = VLAN priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_5	00 = All Frame can be received by this port, including untagged and tagged frames. 01 = Only frame with tag can be received by this port. 10 = Only frame untagged can be received by this port, including no VLAN and priority VLAN. 11 = Reserved
0	RO	0	RESERVED	

5.5.20 PORT6_VLAN_CTRL0

Address offset: 0x0450

Table 5-101 summarizes the port 6 VLAN control 0 register.

Table 5-101 PORT6_VLAN_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:29	R/W	0	ING_PORT_CPRI_6	Port default CVLAN priority for received frames.
28	RO	0	RESERVED	
27:16	R/W	0X1	PORT_DEFAULT_CVID_6	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	ING_PORT_SPRI_6	Port default SVLAN priority for received frames.
12	RO	0	RESERVED	
11:0	R/W	0X1	PORT_DEFAULT_SVID_6	Port default VID. This field is used as tagged VID added to untagged frames when transmitted from this port.

5.5.21 PORT6_VLAN_CTRL1

Address offset: 0x0454

Table 5-102 summarizes the port 6 VLAN control 1 register.

Table 5-102 PORT6_VLAN_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:15	RO	0	RESERVED	
14	R/W	0	EG_VLAN_TYPE_6	0 = All Frames can be sent out. 1 = Only tagged frames can be sent out.
13:12	R/W	3	EG_VLAN_MODE_6	Egress VLAN mode. 00 = Egress transmits frames unmodified 01 = Egress transmits frames without VLAN 10 = Egress transmits frames with VLAN 11 = Untouched
11	RO	0	RESERVED	
10	R/W	0	SPCHECK_EN_6	1 = L3 source port check enable
9	R/W	0	CORE_PORT_EN_6	0 = Edge port 1 = Core port
8	R/W	0	FORCE_DEFAULT_VID_EN_6	0 = Use frame tag only. 1 = Force to use port default VID and priority for received frame, when 802.1q mode is not disable.
7	R/W	0	PORT_TLS_MODE_6	0 = Port work at NON-TLS mode 1 = Port work at TLS mode
6	R/W	1	PORT_VLAN_PROP_EN_6	1 = Enable part-based VLAN propagate function.
5	R/W	0	PORT_CLONE_EN_6	0 = Enable port replace 1 = Enable port clone
4	R/W	0	VLAN_PRI_PRO_EN_6	1 = VLAN priority propagation enable
3:2	R/W	0	ING_VLAN_MODE_6	00 = All frame can be received by this port, including untagged and tagged frames. 01 = Only frame with tag can be received by this port. 10 = Only frame untagged can be received by this port, including no VLAN and priority VLAN. 11 = Reserved
0	RO	0	RESERVED	

5.5.22 IPV4_PRI_BASE_ADDR

Address offset: 0x0470

Table 5-103 summarizes the IPv4 private base address register.

Table 5-103 IPV4_PRI_BASE_ADDR bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	32'hC0A80000	IPV4_PRI_BASE_ADDR	Private IPv4 base address

5.5.23 IPV4_PRI_BASE_ADDR_MASK

Address offset: 0x0474

Table 5-104 summarizes the IPv4 private base address mask register.

Table 5-104 IPV4_PRI_BASE_ADDR_MASK bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	32'hFFFF0000	IPV4_PRI_BASE_ADDR_MASK	Private IPv4 subnet mask

5.6 Lookup register (offset range: 0x0600–0x0718)

Table 5-105 summarizes the lookup registers.

Table 5-105 Lookup register summary

Name	Offset range
ATU data register	0x0600–0x0608
ATU function register	0x060C
VTU function register	0x0610–0x0614
ARL control register	0x0618
Global forward control register	0x0620–0x0624
Global learn limit control	0x0628
TOS priority mapping register	0x0630–0x064C
VLAN priority to priority map register	0x0650
Loop check result	0x0654
Port0 lookup control register	0x0660
Port0 priority control register	0x0664
Port0 learn limit control register	0x0668
Port1 lookup control register	0x066C
Port1 priority control register	0x0670
Port1 learn limit control register	0x0674
Port2 lookup control register	0x0678
Port2 priority control register	0x067C
Port2 learn limit control register	0x0680
Port3 lookup control register	0x0684
Port3 priority control register	0x0688
Port3 learn limit control register	0x068C
Port4 lookup control register	0x0690

Table 5-105 Lookup register summary (cont.)

Name	Offset range
Port4 priority control register	0x0694
Port4 learn limit control register	0x0698
Port5 lookup control register	0x069C
Port5 priority control register	0x06A0
Port5 learn limit control register	0x06A4
Port6 lookup control register	0x06A8
Port6 priority control register	0x06AC
Port6 learn limit control register	0x06B0
Trunk control registers	
Trunk control0 register	0x0700
Trunk control1 register	0x0704
Trunk control2 register	0x0708
ACL registers	
ACL forward source filter register 0	0x0710
ACL forward source filter register 1	0x0714
ACL forward source filter register 2	0x0718

5.6.1 ATU_DATA0

Address offset: 0x0600

Table 5-106 summarizes the ATU data 0 register.

Table 5-106 ATU_DATA0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ATU_MAC_ADDR0	MAC address bits[31:0]

5.6.2 ATU_DATA1

Address offset: 0x0604

Table 5-107 summarizes the ATU data 1 register.

Table 5-107 ATU_DATA1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/WW	0	ATU_HASH_HIGH_ADDR	MAC hash address maximum bit use for Get Next
30	R/WW	0	ATU_SA_DROP_EN	Drop packet enable when source address is in this entry. If this bit is set to 1, the packet with SA of this entry is dropped.
29	R/WW	0	ATU_MIRROR_EN	0 = Packets is send to destination port only. 1 = Packets is send to mirror and destination port.
28	R/WW	0	ATU_PRI_OVER_EN	Priority override enable 1 = ATU_PRI can override any other priority determined by the frame's data.
27	R/WW	0	ATU_SVL_ENTRY	0 = IVL learned 1 = SVL learned
26:24	R/WW	0	ATU_PRI	This priority bits may be used as frame's priority when PRI_OVER_EN is set to one.
23	R/WW	0	ATU_CROSS_PORT_STATE_EN	1 = ATU_CROSS_PORT_STATE enable
22:16	R/WW	0	ATU_DES_PORT	These bits indicate which ports are associated with this MAC address when they are set to 1. Bit[16] is assigned to port0, bit[17] to port1, and bit[18] to port2,etc
15:0	R/WW	0	ATU_MAC_ADDR1	MAC address bits[47:32]

5.6.3 ATU_DATA2

Address offset: 0x0608

Table 5-108 summarizes the ATU data 2 register.

Table 5-108 TU_DATA2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	R/W	0	RESERVED	
20	R/W	0	WHITE_LIST_EN	If the ARL entry is white list (ATU_STATUS = 4'hf and WHITE_LIST_EN is 1'b1), this entry can be updated when this source MAC address coming from other port.
19:8	R/W	0	ATU_VID	This MAC address is the member of ATU_VID group.
7	R/W	0	ATU_SHORT_LOOP	If learn engine find source port mismatch then set to 1, loop check engine clear it.
6	R/W	0	ATU_COPY_TO_CPU	1 = Packet received with this address is copied to CPU port.

Table 5-108 TU_DATA2 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
5	R/W	0	ATU_REDIRECT_TO_CPU	1 = Packet received with this address is redirected to CPU port. If no CPU connected to switch, this frame is discarded.
4	R/W	0	ATU_LEAKY_EN	1 = Use leaky VLAN enable for this MAC address This bit can be used for unicast and multicast frame, control by ARL_UNI_LEAKY_EN and ARL_MULTI_LEAKY_EN.
3:0	R/W	0	ATU_STATUS	4'h0: Entry is empty 4'h1–4'h7: Entry is dynamic and valid. 4'h8–4'hE: Entry is dynamic and valid, can be age but can not be changed by any other address. 4'hF: Entry is static and is not aged or changed by hardware.

5.6.4 ATU_FUNC_REG

Address offset: 0x060C

Table 5-109 summarizes the ATU function register.

Table 5-109 ATU_FUNC_REG bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/WSC	0	AT_BUSY	Depend: AT_DONE, address table busy. This bit must be set to 1 to start an AT operation and cleared to 0 by hardware after the operation is done. If this bit is 1 on read, CPU can not request another operation.
30:25	RO	0	RESERVED	
24:22	R/W	0	TRUNK_PORT_NUM	Trunk port number. When CPU function is change trunk port, the AT_PORT_NUM in ARL bitmap is changed to TRUNK_PORT_NUM.
21	RO	0	RESERVED	
20:16	R/W	0	ATU_INDEX	If ATU_TYPE is reserved ATU entry, this index is the address of reserved ATU entry.
15	R/W	0	AT_VID_EN	1 = When CPU function is Get Next, the VID in the valid ARL entry must be equal to the VID set.
14	R/W	0	AT_PORT_EN	1 = When CPU function is Get Next, the AT_PORT_NUM must be in the destination port in the valid ARL entry.
13	R/W	0	AT_MULTI_EN	0 = All entries. 1 = When CPU function is Get Next, the high bytes of MAC address in the valid ARL entry must be 0x01005E or 0x3333.

Table 5-109 ATU_FUNC_REG bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
12	R/W	0	AT_FULL_VIO	ARL table full violation. This bit is set to 1 if the ARL table is full when CPU want to add a new entry to ARL table, and also be set to 1 if the ARL table is empty when CPU want to purge an entry to ARL table.
11:8	R/W	0	AT_PORT_NUM	Port number to be flushed. If AT_FUNC is set to 0101, lookup module must flush all unicast entries for the port. (or flush the port from ARL table)
7:6	RO	0	RESERVED	
5	R/W	0	ATU_TYPE	0 = Normal ATU entry 1 = Reserved ATU entry
4	R/W	0	FLUSH_STATIC_EN	1 = When AT_FUNC set to 101, static entry in ARL table can be flushed. 0 = When AT_FUNC set to 101, only flush dynamic entry in ARL table.
3:0	R/W	0	AT_FUNC	Address table operate function: 0000 = No operation. 0001 = Flush all entries. 0010 = Load an entry. If these bits are set to 010, CPU want to load an entry into ARL table. 0011 = Purge an entry. If these bits are set to 011, CPU want to purge an entry from ARL table. 0100 = Flush all unlocked entries in ARL. 0101 = Flush one port from ARL table 0110 = Get next valid or static entry in ARL table. If address and AT_STATUS and VID are all zero, hardware searches the first valid entry from entry0. If address is set to zero and AT_STATUS is not zero, hardware searches next valid entry from entry which address is 48'h0. If hardware return back with address and AT_STATUS and VID all zero, there's no other next valid entry in ARL table. 0111 = Search MAC address 1000 = Change trunk port

5.6.5 VTU_FUNC_REG0

Address offset: 0x0610

Table 5-110 summarizes the VTU function register 0.

Table 5-110 VTU_FUNC_REG0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	RO	0	RESERVED	
20	R/WW	0	VTU_VALID	0 = Entry is empty 1 = Entry is valid
19	R/WW	0	VTU_IVL_EN	0 = VID is used to SVL, VID replaced by 0 when search MAC address. 1 = VID is used to IVL
18	R/WW	0	VTU_LEARN_LOOKUP_DIS	0 = Normal operation about learn and final DP 1 = Not learn and not use ARL table DP to calculate final DP, but use UNI flood DP as ARL DP to calculate DP
17:4	R/WW	0	VTU_EG_VLAN_MODE	Bits[5:4] for port0, [7:6] for port1 ... [17:16] for port6 00 = Unmodified 01 = Untagged 10 = Tagged 11 = Not member
3	R/WW	0	VTU_PRI_OVER_EN	VLAN priority override enable
2:0	R/WW	0	VTU_PRI	This priority bits may be used as frame's priority when VTU_PRI_OVER_EN set to 1.

5.6.6 VTU_FUNC_REG1

Address offset: 0x0614

Table 5-111 summarizes the VTU function register 1.

Table 5-111 VTU_FUNC_REG1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/WSC	0	VT_BUSY	Depend: VT_DONE, VLAN table busy. This bit must be set to 1 to start a VT operation and cleared to zero after operation done. If this bit is set to 1, CPU can not request another operation.
30:28	RO	0	RESERVED	
27:16	R/WW	0	VID	Depend: VT_DONE, VT_CSR_VID[11:0], value of VLAN ID to be added or purged.
15:12	RO	0	RESERVED	
11:8	R/W	0	VT_PORT_NUM	Port number
7:5	RO	0	RESERVED	
4	R/OC	0	VT_FULL_VIO	VLAN table full violation. This bit is set to 1 if the VLAN table is full when CPU want to add a new VID to VLAN table.

Table 5-111 VTU_FUNC_REG1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
3	RO	0	RESERVED	
2:0	R/W	0	VT_FUNC	<p>VLAN table operate function.</p> <p>000 = No operation.</p> <p>001 = Flush all entries.</p> <p>010 = Load an entry. If these bits are set to 3'b010, CPU loads an entry into VLAN table.</p> <p>011 = Purge an entry. If these bits are set to 3'b011, CPU purges an entry from VLAN table.</p> <p>100 = Remove an port from VLAN table. The port number which needs to be removed is indicated in VT_PORT_NUM.</p> <p>101 = Get next</p> <p>If VID is 12'b0 and VT_BUSY is set by software, hardware searches the first valid entry in VLAN table.</p> <p>If VID is 12'b0 and VT_BUSY is reset by hardware, there's no valid entry from VID set by software.</p> <p>110 = Read one entry</p>

5.6.7 ARL_CTRL

Address offset: 0x0618

Table 5-112 summarizes the ARL control register.

Table 5-112 ARL_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	1	INVALID_VLAN_IVL_SVL	<p>0 = SVL mode</p> <p>1 = IVL mode</p> <p>The ARL searching mode when VLAN entry lookup is invalid.</p>
30	R/W	1	LEARN_CHANGE_EN	<p>0 = If hash violation occur when learning, no new address be learned to ARL.</p> <p>1 = Enable new MAC address change old one if hash violation occur when learning</p>
29	R/W	0	IGMP_JOIN_LEAKY_EN	<p>IGMP join address leaky VLAN enable</p> <p>0 = IGMP join address needn't be set to LEAKY_EN in ARL table, bit[68] in ATU entry is set to 0.</p> <p>1 = IGMP join address is set to LEAKY_EN in ARL table, bit[68] in ATU entry is set to 1.</p>
28	R/W	1	IGMP_JOIN_NEW_EN	<p>1 = Enable hardware add new address to ARL table when received IGMP/MLD join frame, and remove address from ARL when received IGMP/MLD leave frame.</p>
27	R/W	0	IGMP_JOIN_PRI_REMAP_EN	<p>Use for IGMP packet learn in ARL table, define DA priority remap enable (ATU[60])</p>

Table 5-112 ARL_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
26:24	R/W	3'b0	IGMP_JOIN_PRI	Use for IGMP packet learn in ARL table, define DA priority (ATU[59:57])
23:20	R/W	4'hE	IGMP_JOIN_STATUS	Use for IGMP packet learn in ARL table, define the status (ATU[67:64])
19	R/W	1	AGE_EN	Enable age operation 1 = Lookup module can age the address in the address table.
18:16	R/W	0	LOOP_CHECK_TIMER	3'h0: Disable loop back check 3'h1: 1 ms 3'h2: 10 ms 3'h3: 100 ms 3'h4: 500 ms 3'h5–3'h7: Reserved
15:0	R/W	'h2B	AGE_TIME	Address table age timer. These bits determine the time that each entry remains valid in the address table, since last accessed. For the time is times 7s, maximum age time is about 10,000 minutes. The default value is 'h2B for five minutes. If AGE_EN is set to 1, these bits shouldn't be set to zero.

5.6.8 GLOBAL_FW_CTRL0

Address offset: 0x0620

Table 5-113 summarizes the global forward control 0 register.

Table 5-113 GLOBAL_FW_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	RO	0	RESERVED	
27:26	R/W	0	ARP_FORWARD_ACT	0 = Redirect to CPU 1 = Copy to CPU 2 = Forward
25:24	R/W	0	SP_NOT_FOUND_ACT	For IP packet 0 = Forward 1 = Drop 2 = To CPU
23:22	R/W	0	ARP_SP_NOT_FOUND_ACT	For ARP packet 0 = Forward 1 = Drop 2 = To CPU
21:20	R/W	0	HASH_MODE	Hash mode for MAC address 0 = crc_16 1 = crc_10

Table 5-113 GLOBAL_FW_CTRL0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
19	R/W	0	ARP_REQ_UNI	The destination port of ARP request is only ROUTER_DP in ARP table.
18	RO	0	RESERVED	
17	R/W	0	NAT_NOT_FOUND_DROP_EN	0 = To CPU 1 = Drop
16	RO	0	RESERVED	
15	RO	0	RESERVED	
14	R/W	0	IGMP_LEAVE_DROP_EN	IGMP/MLD leave packet. After updated the port map of ARL (IGMP/MLD group address). If port map in ARL is not empty, 0 = Forward to IGMP_JOIN_LEAVE_DP 1 = Drop this packet
13	R/W	0	ARL_UNI_LEAKY_EN	0 = Ignore LEAKY_EN bit in ARL table to control unicast frame leaky VLAN. Only use port-based UNI_LEAKY_EN to control unicast frame leaky VLAN. 1 = Use LEAKY_EN bit in ARL table to control unicast frame leaky VLAN, and ignore UNI_LEAKY_EN.
12	R/W	0	ARL_MULTI_LEAKY_EN	0 = Ignore LEAKY_EN bit in ARL table to control multicast frame leaky VLAN. Only use port-based MULTI_LEAKY_EN to control multicast frame leaky VLAN. 1 = Use LEAKY_EN bit in ARL table to control multicast frame leaky VLAN, and ignore MULTI_LEAKY_EN.
11	R/W	1	MANAGE_VID_VIO_DROP_EN	0 = Management frame transmit out if VLAN violation occurs. 1 = Management frame is drop if VLAN violation occurs.
10	R/W	0	CPU_PORT_EN	0 = No CPU connect to switch 1 = CPU is connected to port0 If this bit is set to 1, HEAD_EN of MAC0 is set to 1.
9	RO	0	RESERVED	
8	R/W	0	PPPOE_REDIRECT_EN	PPPoE discovery frame redirect to CPU enable. If this bit is set to 1, PPPoE discovery frame is redirected to CPU port. If this bit set to 0, PPPoE discovery frame is transmitted as normal frame.
7:4	R/W	0xF	MIRROR_PORT_NUM	Port number which packet is mirrored to. 4'h0 is port0, 4'h1 is port1, etc. If value is more than 6, no mirror port connected to switch.

Table 5-113 GLOBAL_FW_CTRL0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
3	R/W	0	IGMP_COPY_EN	0 = QM redirects IGMP/MLD frame to CPU port. 1 = QM copies IGMP/MLD frame to CPU port. This IGMP does not include the IGMP join/leave packet
2	R/W	0	RIP_COPY_EN	0 = Do not copy RIPv1 frame to CPU 1 = Copy RIPv1 frame to CPU
1	R/W	0	RESERVED	
0	R/W	0	EAPOL_REDIRECT_EN	0 = 802.1x frame copy to CPU 1 = 802.1x frame redirect to CPU

5.6.9 GLOBAL_FW_CTRL1

Address offset: 0x0624

Table 5-114 summarizes the global forward control 1 register.

Table 5-114 GLOBAL_FW_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:14	RO	0	RESERVED	
13	R/W	0	GOL_SA_LEARN_LIMIT_DROP_EN	0 = If SA is not in ARL table or SA in ARL but port member is not the source port, packet is redirected to CPU when learned MAC address counter is equal to GOL_SA_LEARN_CNT. 1 = If SA is not in ARL table, packet is dropped when global learned MAC address counter is equal to GOL_SA_LEARN_CNT.
12	R/W	0	GOL_SA_LEARN_LIMIT_EN	1 = Global SA learn limit enable
11:0	R/W	0	GOL_SA_LEARN_CNT	Global MAC address can be learned to ARL. When learn new MAC address + 1, age - 1.

5.6.10 GOL_LEARN_LIMIT

Address offset: 0x0628

Table 5-115 summarizes the global learn limit control register.

Table 5-115 GOL_LEARN_LIMIT bit description

Bits	R/W	Initial value	Mnemonic	Description
31:13	RO	0	RESERVED	
12	R/W	0	GOL_SA_LEARN_LIMIT_EN	1 = SA learn limit enable.
11	R/W	0	GOL_SA_LEARN_LIMIT_DROP_EN	0 = If SA is not in ARL table or SA in ARL but port member is not the source port, packet is redirected to CPU when learned MAC address counter is equal to GOL_SA_LEARN_CNT 1 = If SA is not in ARL table or SA in ARL but port member is not the source port, packet is dropped when learned MAC address counter is equal to GOL_SA_LEARN_CNT
10:0	R/W	0	GOL_SA_LEARN_CNT	The MAC address can be learned and written to the ARL table — only dynamic entry is counted. 0: Indicate the MAC limit number is 0 1: Indicate the MAC limit number is 1 2: Indicate the MAC limit number is 2 ... and so on... until: 2048: Indicate the MAC limit is 2048

5.6.11 TOS_PRI_MAP_REG0

Address offset: 0x0630

Table 5-116 summarizes the TOS/TC priority mapping register 0.

Table 5-116 TOS_PRI_MAP_REG0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0X1C	See bits[3:0]
27:24	R/W	0	TOS_MAP_0X18	See bits[3:0]
23:20	R/W	0	TOS_MAP_0X14	See bits[3:0]
19:16	R/W	0	TOS_MAP_0X10	See bits[3:0]
15:12	R/W	0	TOS_MAP_0X0C	See bits[3:0]
11:8	R/W	0	TOS_MAP_0X08	See bits[3:0]
7:4	R/W	0	TOS_MAP_0X04	3:0 DEI
3:0	R/W	0	TOS_MAP_0X00	2:0 Priority

5.6.12 TOS_PRI_MAP_REG1

Address offset: 0x0634

Table 5-117 summarizes the TOS/TC priority mapping register 1.

Table 5-117 TOS_PRI_MAP_REG1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0X3C	See bits[3:0] of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0X38	See bits[3:0] of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0X34	See bits[3:0] of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0X30	See bits[3:0] of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0X2C	See bits[3:0] of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0X28	See bits[3:0] of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0X24	See bits[3:0] of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0X20	

5.6.13 TOS_PRI_MAP_REG2

Address offset: 0x0638

Table 5-118 summarizes the TOS/TC priority mapping register 2.

Table 5-118 TOS_PRI_MAP_REG2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0X5C	See bits[3:0] of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0X58	See bits[3:0] of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0X54	See bits[3:0] of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0X50	See bits[3:0] of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0X4C	See bits[3:0] of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0X48	See bits[3:0] of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0X44	See bits[3:0] of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0X40	

5.6.14 TOS_PRI_MAP_REG3

Address offset: 0x063C

Table 5-119 summarizes the TOS/TC priority mapping register 3.

Table 5-119 TOS_PRI_MAP_REG3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0X7C	See bits[3:0] of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0X78	See bits[3:0] of TOS_PRI_MAP_REG0

Table 5-119 TOS_PRI_MAP_REG3 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
23:20	R/W	0	TOS_MAP_0X74	See bits[3:0] of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0X70	See bits[3:0] of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0X6C	See bits[3:0] of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0X68	See bits[3:0] of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0X64	See bits[3:0] of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0X60	See bits[3:0] of TOS_PRI_MAP_REG0

5.6.15 TOS_PRI_MAP_REG4

Address offset: 0x0640

Table 5-120 summarizes the TOS/TC priority mapping register 4.

Table 5-120 TOS_PRI_MAP_REG4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0X9C	See bits[3:0] of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0X98	See bits[3:0] of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0X94	See bits[3:0] of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0X90	See bits[3:0] of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0X8C	See bits[3:0] of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0X88	See bits[3:0] of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0X84	See bits[3:0] of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0X80	See bits[3:0] of TOS_PRI_MAP_REG0

5.6.16 TOS_PRI_MAP_REG5

Address offset: 0x0644

Table 5-121 summarizes the TOS/TC priority mapping register 5.

Table 5-121 TOS_PRI_MAP_REG5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0XBC	See bits[3:0] of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0XB8	See bits[3:0] of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0XB4	See bits[3:0] of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0XB0	See bits[3:0] of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0XAC	See bits[3:0] of TOS_PRI_MAP_REG0

Table 5-121 TOS_PRI_MAP_REG5 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
11:8	R/W	0	TOS_MAP_0XA8	See bits[3:0] of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0XA4	See bits[3:0] of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0XA0	See bits[3:0] of TOS_PRI_MAP_REG0

5.6.17 TOS_PRI_MAP_REG6

Address offset: 0x0648

Table 5-122 summarizes the TOS/TC priority mapping register 6.

Table 5-122 TOS_PRI_MAP_REG6 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0XDC	See bits[3:0] of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0XD8	See bits[3:0] of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0XD4	See bits[3:0] of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0XD0	See bits[3:0] of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0XCC	See bits[3:0] of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0XC8	See bits[3:0] of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0XC4	See bits[3:0] of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0XC0	See bits[3:0] of TOS_PRI_MAP_REG0

5.6.18 TOS_PRI_MAP_REG7

Address offset: 0x064C

Table 5-123 summarizes the TOS/TC priority mapping register 7.

Table 5-123 TOS_PRI_MAP_REG7 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	R/W	0	TOS_MAP_0XFC	See bits[3:0] of TOS_PRI_MAP_REG0
27:24	R/W	0	TOS_MAP_0XF8	See bits[3:0] of TOS_PRI_MAP_REG0
23:20	R/W	0	TOS_MAP_0XF4	See bits[3:0] of TOS_PRI_MAP_REG0
19:16	R/W	0	TOS_MAP_0XF0	See bits[3:0] of TOS_PRI_MAP_REG0
15:12	R/W	0	TOS_MAP_0XEC	See bits[3:0] of TOS_PRI_MAP_REG0
11:8	R/W	0	TOS_MAP_0XE8	See bits[3:0] of TOS_PRI_MAP_REG0
7:4	R/W	0	TOS_MAP_0XE4	See bits[3:0] of TOS_PRI_MAP_REG0
3:0	R/W	0	TOS_MAP_0XE0	See bits[3:0] of TOS_PRI_MAP_REG0

5.6.19 VLAN_PRI_MAP_REG0

Address offset: 0x0650

Table 5-124 summarizes the VLAN priority to priority mapping register 0.

Table 5-124 VLAN_PRI_MAP_REG0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	R/W	7	VLAN_MAP_0X7	See bits[3:0] of VLAN_PRI_MAP_REG0
27:24	R/W	6	VLAN_MAP_0X6	See bits[3:0] of VLAN_PRI_MAP_REG0
23:20	R/W	5	VLAN_MAP_0X5	See bits[3:0] of VLAN_PRI_MAP_REG0
19:16	R/W	4	VLAN_MAP_0X4	See bits[3:0] of VLAN_PRI_MAP_REG0
15:12	R/W	3	VLAN_MAP_0X3	See bits[3:0] of VLAN_PRI_MAP_REG0
11:8	R/W	2	VLAN_MAP_0X2	See bits[3:0] of VLAN_PRI_MAP_REG0
7:4	R/W	1	VLAN_MAP_0X1	See bits[3:0] of VLAN_PRI_MAP_REG0
3:0	R/W	0	VLAN_MAP_0X0	[3]: DEI [2:0] Priority

5.6.20 LOOP_CHECK_RESULT

Address offset: 0x0654

Table 5-125 summarizes the loop check result register.

Table 5-125 LOOP_CHECK_RESULT bit description

Bits	R/W	Initial value	Mnemonic	Description
31:8	RO	0	RESERVED	
7:4	RO	0	PORT_NUM_NEW	When hardware checked loop occur, these bits indicate MAC address new port number.
3:0	RO	0	PORT_NUM_OLD	When hardware checked loop occur, these bits indicate MAC address old port number.

5.6.21 PORT0_LOOKUP_CTRL

Address offset: 0x0660

Table 5-126 summarizes the port 0 lookup control register.

Table 5-126 PORT0_LOOKUP_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_0	1 = Drop the multicast packet from this port. Do not drop IGMP/MLD join/leave and special DIP packet.
30:29	RO	0	RESERVED	
28	R/W	0	UNI_LEAKY_EN_0	Unicast frame leaky VLAN enable. Use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKY_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. If MAC receives unicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based and 802.1q).
27	R/W	0	MULTI_LEAKY_EN_0	Use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. If MAC receives multicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_0	0 = ARP frame can not cross VLAN ingress port mirror. If this bit is set to 1, all packets received from this port are copied to mirror port. 1 = If MAC receive ARP frame from this port, it can cross all VLAN (include part-based VLAN and 802.1q).
25	R/W	0	ING_MIRROR_EN_0	Ingress port mirror. If this bit is set to 1, all packets received from this port is copied to mirror port.
24	RO	0	RESERVED	
23	RO	0	RESERVED	
22	RO	0	RESERVED	
21	R/W	0	PORT_LOOPBACK_EN_0	0 = Normal forwarding 1 = Loop back. Packet sent in from this port is sent out from the same port. This packet is not sent to other ports.
20	R/W	1	LEARN_EN_0	Enable learn operation 0 = Do not learn new MAC address to ARL table 1 = Enable hardware learn new MAC address into ARL table.
19	RO	0	RESERVED	

Table 5-126 PORT0_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
18:16	R/W	3'h4	PORT_STATE_0	<p>Port state. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree.</p> <p>000 = Disable mode. The port is completely disabled, and can not receive or transmit any frames.</p> <p>001 = Blocking mode. In this state, the port forwards received management frames to the designed port only. Any other frames can not be transmitted or received by the port, and without learning any SA address.</p> <p>010 = Listening mode. In this state, the port receives and transmits only management frames, but without learning any SA address. Any other frames can not be transmitted or received by the port.</p> <p>011 = Learning mode. In this state, the port learns all SA, and discards all frames except management frames, and only management frames allowed to be transmitted out.</p> <p>100 = Forward mode. In this state, the port learns all SA, transmits and receives all frames like normal.</p>
15	RO	0	RESERVED	
14:12	RO	0	RESERVED	
11	RO	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_0	1 = Force to use port-based VLAN enable. If this bit is set to 1, use port-based VLAN & VLAN table result to determine destination port.
9:8	R/W	00	VLAN_MODE_0	<p>802.1q mode for this port.</p> <p>00 = 802.1q disable. Use port-based VLAN only.</p> <p>01 = Fallback. Enable 802.1q for all received frames. Do not discard ingress membership violation and use the port-based VLAN if the frame's VID is not contained in VLAN table.</p> <p>10 = Check. Enable 802.1q for all received frames. Do not discard ingress membership violation but discard frames which VID is not contained in VLAN table.</p> <p>11 = Secure. Enable 802.1q for all received frames. Discard frames with ingress membership violation or whose VID is not contained in the VLAN table.</p>
7	RO	0	RESERVED	
6:0	R/W	'h7E	PORT_VID_MEM_0	Port-based VLAN member. Each bit restricts which port can send frames to. To send frames to port0, bit[16] must be set to 1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

5.6.22 PORT0_PRI_CTRL

Address offset: 0x0664

Table 5-127 summarizes the port 0 priority control register.

Table 5-127 PORT0_PRI_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	RO	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_0	Enable egress MAC-based VLAN
19	RO	0	RESERVED	
18	R/W	0	DA_PRI_EN_0	1 = DA priority can be used for QoS.
17	R/W	0	VLAN_PRI_EN_0	1= VLAN priority can be used for QoS.
16	R/W	0	IP_PRI_EN_0	1 = TOS/TC can be used for QoS.
15:8	RO	0	RESERVED	
7:6	R/W	0	DA_PRI_SEL_0	DA priority selected level for QoS. There are five levels of priority for QoS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_0	DA priority selected level for QoS.
3:2	R/W	2	IP_PRI_SEL_0	IP priority selected level for QoS.
1:0	RO	0	RESERVED	

5.6.23 PORT0_LEARN_LIMIT

Address offset: 0x0668

Table 5-128 summarizes the port 0 learn limit control register.

Table 5-128 PORT0_LEARN_LIMIT bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_0	Drop or redirect the ingress frame to CPU when new group address coming but learned group address already reach the limitation
28	R/W	0	SA_LEARN_LIMIT_DROP_EN_0	Drop or redirect the ingress frame to CPU when new SA coming but learned SA already reach the limitation
27	R/W	0	IGMP_LEARN_LIMIT_EN_0	1 = IGMP Learn Limit enable.
26:16	R/W	0	IGMP_JOIN_CNT_0	Hardware join IGMP. When join new entry or new port to IGMP + 1, leave or age - 1.

Table 5-128 PORT0_LEARN_LIMIT bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
15:12	R/W	7	SA_LEARN_STATUS_0	If less than 0x7, dynamic can be fresh to setting value and age.
11	R/W	0	SA_LEARN_LIMIT_EN_0	1 = SA learn limit enable
10:0	R/W	0	SA_LEARN_CNT_0	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: Indicate the MAC limit number is 0 1: Indicate the MAC limit number is 1 2: Indicate the MAC limit number is 2 ... and so on... until: 1024: Indicate the MAC limit is 1024

5.6.24 PORT1_LOOKUP_CTRL

Address offset: 0x066C

Table 5-129 summarizes the port 1 lookup control register.

Table 5-129 PORT1_LOOKUP_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_1	1 = Drop the multicast packet from this port. Do not drop IGMP/MLD join/leave and Special DIP packet.
30:29	RO	0	RESERVED	
28	R/W	0	UNI_LEAKY_EN_1	Unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. If MAC receive unicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based and 802.1q).

Table 5-129 PORT1_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
27	R/W	0	MULTI_LEAKY_EN_1	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. If MAC receive multicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_1	0 = ARP frame can not cross VLAN 1 = If MAC receive ARP frame from this port, it can cross all VLAN (include part-based VLAN and 802.1q).
25	R/W	0	ING_MIRROR_EN_1	Ingress port mirror. If this bit is set to 1, all packets received from this port is copied to mirror port.
24:22	RO	0	RESERVED	
21	R/W	0	PORT_LOOPBACK_EN_1	0 = Normal forwarding 1 = Loop back. Packet sent in from this port is sent out from the same port. This packet is not sent to other ports
20	R/W	1	LEARN_EN_1	Enable learn operation 0 = Do not learn new MAC address to ARL table 1 = Enable hardware learn new MAC address into ARL table.
19	RO	0	RESERVED	
18:16	R/W	3'h4	PORT_STATE_1	Port state. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree. 000 = Disable mode. The port is completely disabled, and can not receive or transmit any frames. 001 = Blocking mode. In this state, the port forwards received management frames to the designed port only. Any other frames can not be transmitted or received by the port, and without learning any SA address. 010 = Listening mode. In this state, the port receives and transmits only management frames, but without learning any SA address. Any other frames can not be transmitted or received by the port. 011 = Learning mode. In this state, the port learns all SA, and discards all frames except management frames, and only management frames allowed to be transmitted out. 100 = Forward mode. In this state, the port learns all SA, transmits and receives all frames like normal.
15:11	RO	0	RESERVED	

Table 5-129 PORT1_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
10	R/W	0	FORCE_PORT_VLAN_EN_1	1 = Force to use part-based VLAN enable. If this bit is set to 1, use part-based VLAN & VLAN table result to determine destination port.
9:8	R/W	00	VLAN_MODE_1	802.1q mode for this port. 00 = 802.1q disable. Use part-based VLAN only. 01 = Fallback. Enable 802.1q for all received frames. Do not discard ingress membership violation and use the part-based VLAN if the frame's VID is not contained in VLAN table. 10 = Check. Enable 802.1q for all received frames. Do not discard ingress membership violation but discard frames which VID is not contained in VLAN table. 11 = Secure. Enable 802.1q for all received frames. Discard frames with ingress membership violation or whose VID is not contained in the VLAN table.
7	RO	0	RESERVED	
6:0	R/W	0h7D	PORT_VID_MEM_1	Port-based VLAN member. Each bit restrict which port can send frames to. To send frames to port0, bit 16 must be set to 1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

5.6.25 PORT1_PRI_CTRL

Address offset: 0x0670

Table 5-130 summarizes the port 1 priority control register.

Table 5-130 PORT1_PRI_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	RO	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_1	Enable egress MAC-based VLAN
19	RO	0	RESERVED	
18	R/W	0	DA_PRI_EN_1	1 = DA priority can be used for QoS.
17	R/W	0	VLAN_PRI_EN_1	1 = VLAN priority can be used for QoS.
16	R/W	0	IP_PRI_EN_1	1 = TOS/TC can be used for QoS.
15:8	RO	0	RESERVED	

Table 5-130 PORT1_PRI_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
7:6	R/W	0	DA_PRI_SEL_1	DA priority selected level for QoS. There are five levels of priority for QoS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_1	
3:2	R/W	2	IP_PRI_SEL_1	DA priority selected level for QoS.
1:0	RO	0	RESERVED	IP priority selected level for QoS.

5.6.26 PORT1_LEARN_LIMIT

Address offset: 0x0674

Table 5-131 summarizes the port 1 learn limit register.

Table 5-131 PORT1_LEARN_LIMIT bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_1	Drop or redirect the ingress frame to CPU when new group address coming but learned group address already reach the limitation
28	R/W	0	SA_LEARN_LIMIT_DROP_EN_1	Drop or redirect the ingress frame to CPU when new SA coming but learned SA already reach the limitation
27	R/W	0	IGMP_LEARN_LIMIT_EN_1	1 = IGMP learn limit enable.
26:16	R/W	0	IGMP_JOIN_CNT_1	Hardware join IGMP. When join new entry or new port to IGMP + 1, leave or age - 1
15:12	R/W	7	SA_LEARN_STATUS_1	If less than 0x7, dynamic can be fresh to setting value and age.
11	R/W	0	SA_LEARN_LIMIT_EN_1	1 = SA learn limit enable.
10:0	R/W	0	SA_LEARN_CNT_1	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: Indicate the MAC limit number is 0 1: Indicate the MAC limit number is 1 2: Indicate the MAC limit number is 2 ... and so on... until: 1024: Indicate the MAC limit is 1024

5.6.27 PORT2_LOOKUP_CTRL

Address offset: 0x0678

Table 5-132 summarizes the port 2 lookup control register.

Table 5-132 PORT2_LOOKUP_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_2	1 = Drop the multicast packet from this port. Do not drop IGMP/MLD join/leave and special DIP packet.
30:29	RO	0	RESERVED	
28	R/W	0	UNI_LEAKY_EN_2	Unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. If MAC receive unicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based and 802.1q).
27	R/W	0	MULTI_LEAKY_EN_2	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. If MAC receive multicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_2	0 = ARP frame can not cross VLAN 1 = If MAC receive ARP frame from this port, it can cross all VLAN (include part-based VLAN and 802.1q).
25	R/W	0	ING_MIRROR_EN_2	Ingress port mirror. If this bit is set to 1, all packets received from this port is copied to mirror port.
24:22	RO	0	RESERVED	
21	R/W	0	PORT_LOOPBACK_EN_2	0 = Normal forwarding 1 = Loop back. Packet sent in from this port is sent out from the same port. This packet is not sent to other ports
20	R/W	1	LEARN_EN_2	Enable learn operation 0 = Not learn new MAC address to ARL table 1 = Enable hardware learn new MAC address into ARL table.

Table 5-132 PORT2_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
19	RO	0	RESERVED	
18:16	R/W	3'h4	PORT_STATE_2	
15	RO	0	RESERVED	
14:12	RO	0	RESERVED	
11	RO	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_2	
9:8	R/W	00	VLAN_MODE_2	802.1q mode for this port. 00 = 802.1q disable. Use part-based VLAN only. 01 = Fallback. Enable 802.1q for all received frames. Do not discard ingress membership violation and use the part-based VLAN if the frame's VID is not contained in VLAN table. 10 = Check. Enable 802.1q for all received frames. Do not discard ingress membership violation but discard frames which VID is not contained in VLAN table. 11 = Secure. Enable 802.1q for all received frames. Discard frames with ingress membership violation or whose VID is not contained in the VLAN table.
7	R/W	0'	RESERVED	
6:0	R/W	h7B	PORT_VID_MEM_2	Port-based VLAN member. Each bit restricts which port can send frames to. To send frames to port0, bit[16] must be set to 1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

5.6.28 PORT2_PRI_CTRL

Address offset: 0x067C

Table 5-133 summarizes the port 2 priority control register.

Table 5-133 PORT2_PRI_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	RO	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_2	Enable egress MAC-based VLAN
19	RO	0	RESERVED	
18	R/W	0	DA_PRI_EN_2	1 = DA priority can be used for QoS.
17	R/W	0	VLAN_PRI_EN_2	1 = VLAN priority can be used for QoS.
16	R/W	0	IP_PRI_EN_2	1 = TOS/TC can be used for QoS.

Table 5-133 PORT2_PRI_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
15:8	RO	0	RESERVED	
7:6	R/W	0	DA_PRI_SEL_2	DA priority selected level for QoS. There are five levels of priority for QoS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_2	DA priority selected level for QoS.
3:2	R/W	2	IP_PRI_SEL_2	IP priority selected level for QoS.
1:0	RO	0	RESERVED	

5.6.29 PORT2_LEARN_LIMIT

Address offset: 0x0680

Table 5-134 summarizes the port 2 learn limit control register.

Table 5-134 PORT2_LEARN_LIMIT bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_2	Drop or redirect the ingress frame to CPU when new group address coming but learned group address already reach the limitation
28	R/W	0	SA_LEARN_LIMIT_DROP_EN_2	Drop or redirect the ingress frame to CPU when new SA coming but learned SA already reach the limitation
27	R/W	0	IGMP_LEARN_LIMIT_EN_2	1 = IGMP learn limit enable.
26:16	R/W	0	IGMP_JOIN_CNT_2	Hardware join IGMP. When join new entry or new port to IGMP + 1, leave or age - 1.
15:12	R/W	7	SA_LEARN_STATUS_2	If less than 0x7, dynamic can be fresh to setting value and age.
11	R/W	0	SA_LEARN_LIMIT_EN_2	1 = SA Learn Limit enable.
10:0	R/W	0	SA_LEARN_CNT_2	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: Indicate the MAC limit number is 0 1: Indicate the MAC limit number is 1 2: Indicate the MAC limit number is 2 ... and so on... until: 1024: Indicate the MAC limit is 1024

5.6.30 PORT3_LOOKUP_CTRL

Address offset: 0x0684

Table 5-135 summarizes the port 3 lookup control register.

Table 5-135 PORT3_LOOKUP_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_3	1 = Drop the multicast packet from this port. Do not drop IGMP/MLD join/leave and Special DIP packet.
30:29	RO	0	RESERVED	
28	R/W	0	UNI_LEAKY_EN_3	Unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN; ignore UNI_LEAKY_EN. If MAC receive unicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based and 802.1q).
27	R/W	0	MULTI_LEAKY_EN_3	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN; ignore MULTI_LEAKY_EN. If MAC receive multicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_3	0 = ARP frame can not cross VLAN 1 = If MAC receive ARP frame from this port, it can cross all VLAN (include part-based VLAN and 802.1q).
25	R/W	0	ING_MIRROR_EN_3	Ingress port mirror. If this bit is set to 1, all packets received from this port is copied to mirror port.
24	RO	0	RESERVED	
23	RO	0	RESERVED	
22	RO	0	RESERVED	
21	R/W	0	PORT_LOOPBACK_EN_3	0 = Normal forwarding 1 = Loop back. Packet sent in from this port is sent out from the same port. This packet is not sent to other ports.

Table 5-135 PORT3_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
20	R/W	1	LEARN_EN_3	Enable learn operation 0 = Do not learn new MAC address to ARL table 1 = Enable hardware learn new MAC address into ARL table.
19	RO	0	RESERVED	
18:16	R/W	3'h4	PORT_STATE_3	Port state. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree. 000 = Disable mode. The port is completely disabled, and can not receive or transmit any frames. 001 = Blocking mode. In this state, the port forwards received management frames to the designed port only. Any other frames can not be transmitted or received by the port, and without learning any SA address. 010 = Listening mode. In this state, the port receives and transmits only management frames, but without learning any SA address. Any other frames can not be transmitted or received by the port. 011 = Learning mode. In this state, the port learns all SA, and discards all frames except management frames, and only management frames allowed to be transmitted out. 100 = Forward mode. In this state, the port learns all SA, transmits and receives all frames like normal.
15	RO	0	RESERVED	
14:12	RO	0	RESERVED	
11	RO	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_3	1 = Force to use part-based VLAN enable. If this bit is set to 1, use part-based VLAN & VLAN table result to determine destination port.
9:8	R/W	00	VLAN_MODE_3	802.1q mode for this port. 00 = 802.1q disable. Use part-based VLAN only. 01 = Fallback. Enable 802.1q for all received frames. Do not discard ingress membership violation and use the part-based VLAN if the frame's VID is not contained in VLAN table. 10 = Check. Enable 802.1q for all received frames. Do not discard ingress membership violation but discard frames which VID is not contained in VLAN table. 11 = Secure. Enable 802.1q for all received frames. Discard frames with ingress membership violation or whose VID is not contained in the VLAN table.

Table 5-135 PORT3_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
7	R/W	0'	RESERVED	
6:0	R/W	h7B	PORT_VID_MEM_3	Port-based VLAN member. Each bit restricts which port can send frames to. To send frames to port0, bit[16] must be set to 1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

5.6.31 PORT3_PRI_CTRL

Address offset: 0x0688

Table 5-136 summarizes the port 3 priority control register.

Table 5-136 PORT3_PRI_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	RO	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_3	Enable egress MAC-based VLAN
19	RO	0	RESERVED	
18	R/W	0	DA_PRI_EN_3	1 = DA priority can be used for QoS.
17	R/W	0	VLAN_PRI_EN_3	1 = VLAN priority can be used for QoS.
16	R/W	0	IP_PRI_EN_3	1 = TOS/TC can be used for QoS.
15:8	RO	0	RESERVED	
7:6	R/W	0	DA_PRI_SEL_3	DA priority selected level for QoS. There are five levels of priority for QoS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_3	DA priority selected level for QoS.
3:2	R/W	2	IP_PRI_SEL_3	IP priority selected level for QoS.
1:0	RO	0	RESERVED	

5.6.32 PORT3_LEARN_LIMIT

Address offset: 0x068C

Table 5-137 summarizes the port 3 learn limit control register.

Table 5-137 PORT3_LEARN_LIMIT bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_3	Drop or redirect the ingress frame to CPU when new group address coming but learned group address already reach the limitation
28	R/W	0	SA_LEARN_LIMIT_DROP_EN_3	Drop or redirect the ingress frame to CPU when new SA coming but learned SA already reach the limitation
27	R/W	0	IGMP_LEARN_LIMIT_EN_3	1 = IGMP learn limit enable.
26:16	R/W	0	IGMP_JOIN_CNT_3	Hardware join IGMP. When join new entry or new port to IGMP + 1, leave or age - 1.
15:12	R/W	7	SA_LEARN_STATUS_3	If less than 0x7, dynamic can be fresh to setting value and age.
11	R/W	0	SA_LEARN_LIMIT_EN_3	1 = SA learn limit enable.
10:0	R/W	0	SA_LEARN_CNT_3	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: Indicate the MAC limit number is 0 1: Indicate the MAC limit number is 1 2: Indicate the MAC limit number is 2 ... and so on... until: 1024: Indicate the MAC limit is 1024

5.6.33 PORT4_LOOKUP_CTRL

Address offset: 0x0690

Table 5-138 summarizes the port 4 lookup control register.

Table 5-138 PORT4_LOOKUP_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_4	1 = Drop the multicast Packet from this port. Do not drop IGMP/MLD join/leave and special DIP packet.
30:29	RO	0	RESERVED	

Table 5-138 PORT4_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
28	R/W	0	UNI_LEAKY_EN_4	Unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKY_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. If MAC receive unicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based and 802.1q).
27	R/W	0	MULTI_LEAKY_EN_4	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. If MAC receive multicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_4	0 = ARP frame can not cross VLAN 1 = If MAC receive ARP frame from this port, it can cross all VLAN (include part-based VLAN and 802.1q).
25	R/W	0	ING_MIRROR_EN_4	Ingress port mirror. If this bit is set to 1, all packets received from this port is copied to mirror port.
24:22	RO	0	RESERVED	
21	R/W	0	PORT_LOOPBACK_EN_4	0 = Normal forwarding 1 = Loop back. Packet sent in from this port is sent out from the same port. This packet is not sent to other ports.
20	R/W	1	LEARN_EN_4	Enable learn operation. 0 = Do not learn new MAC address to ARL table 1 = Enable hardware learn new MAC address into ARL table.
19	RO	0	RESERVED	

Table 5-138 PORT4_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
18:16	RO	3'h4	PORT_STATE_4	<p>Port state. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree.</p> <p>000 = Disable mode. The port is completely disable, and can not receive or transmit any frames.</p> <p>001 = Blocking mode. In this state, the port forwards received management frames to the designed port only. Any other frames can not be transmitted or received by the port, and without learning any SA address.</p> <p>010 = Listening mode. In this state, the port receives and transmits only management frames, but without learning any SA address. Any other frames can not be transmitted or received by the port.</p> <p>011 = Learning mode. In this state, the port learns all SA, and discards all frames except management frames, and only management frames allowed to be transmitted out.</p> <p>100 = Forward mode. In this state, the port learns all SA, transmits and receives all frames like normal.</p>
15:12	RO	0	RESERVED	
11	R/W	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_4	1 = Force to use part-based VLAN enable. If this bit is set to 1, use part-based VLAN & VLAN table result to determine destination port.
9:8	R/W	2'0	VLAN_MODE_4	<p>802.1q mode for this port.</p> <p>00 = 802.1q disable. Use part-based VLAN only.</p> <p>01 = Fallback. Enable 802.1q for all received frames. Do not discard ingress membership violation and use the part-based VLAN if the frame's VID is not contained in VLAN table.</p> <p>10 = Check. Enable 802.1q for all received frames. Do not discard ingress membership violation but discard frames which VID is not contained in VLAN table.</p> <p>11 = Secure. Enable 802.1q for all received frames. Discard frames with ingress membership violation or whose VID is not contained in the VLAN table.</p>
7	RO	'h6F	RESERVED	
6:0	R/W	b00	PORT_VID_MEM_4	Port-based VLAN member. Each bit restricts which port can send frames to. To send frames to port0, bit[16] must be set to 1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

5.6.34 PORT4_PRI_CTRL

Address offset: 0x0694

Table 5-139 summarizes the port 4 priority control register.

Table 5-139 PORT4_PRI_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	RO	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_4	Enable egress MAC-based VLAN
19	RO	0	RESERVED	
18	R/W	0	DA_PRI_EN_4	DA priority selected level for QoS. There are five levels of priority for QoS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
17	R/W	0	VLAN_PRI_EN_4	DA priority selected level for QoS.
16	R/W	0	IP_PRI_EN_4	IP priority selected level for QoS.
15:8	RO	0	RESERVED	
7:6	R/W	0	DA_PRI_SEL_4	DA priority selected level for QoS. There are five levels of priority for QoS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_4	DA priority selected level for QoS.
3:2	R/W	2	IP_PRI_SEL_4	IP priority selected level for QoS.
1:0	RO	0	RESERVED	

5.6.35 PORT4_LEARN_LIMIT

Address offset: 0x0698

Table 5-140 summarizes the port 4 learn limit control register.

Table 5-140 PORT4_LEARN_LIMIT bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_4	Drop or redirect the ingress frame to CPU when new group address coming but learned group address already reach the limitation
28	R/W	0	SA_LEARN_LIMIT_DROP_EN_4	Drop or redirect the ingress frame to CPU when new SA coming but learned SA already reach the limitation

Table 5-140 PORT4_LEARN_LIMIT bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
27	R/W	0	IGMP_LEARN_LIMIT_EN_4	1 = IGMP Learn Limit enable.
26:16	R/W	0	IGMP_JOIN_CNT_4	Hardware join IGMP. When joining new entry or new port to IGMP + 1, leave or AGE - 1.
15:12	R/W	7	SA_LEARN_STATUS_4	If less than 0x7, dynamic can be refreshed to setting value and age
11	R/W	0	SA_LEARN_LIMIT_EN_4	1 = SA learn limit enable.
10:0	R/W	0	SA_LEARN_CNT_4	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: Indicate the MAC limit number is 0 1: Indicate the MAC limit number is 1 2: Indicate the MAC limit number is 2 ... and so on... until: 1024: Indicate the MAC limit is 1024

5.6.36 PORT5_LOOKUP_CTRL

Address offset: 0x069C

Table 5-141 summarizes the port 5 lookup control register.

Table 5-141 PORT5_LOOKUP_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_5	1 = Drop the multicast Packet from this port. Do not drop IGMP/MLD join/leave and Special DIP packet.
30:29	RO	0	RESERVED	
28	R/W	0	UNI_LEAKY_EN_5	Unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. If MAC receive unicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based and 802.1q).

Table 5-141 PORT5_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
27	R/W	0	MULTI_LEAKY_EN_5	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. If MAC receive multicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_5	0 = ARP frame can not cross VLAN 1 = If MAC receives ARP frame from this port, it can cross all VLAN (include part-based VLAN and 802.1q).
25	R/W	0	ING_MIRROR_EN_5	Ingress port mirror. If this bit is set to 1, all packets received from this port is copied to mirror port.
24	RO	0	RESERVED	
23	RO	0	RESERVED	
22	RO	0	RESERVED	
21	R/W	0	PORT_LOOPBACK_EN_5	0 = Normal forwarding 1 = Loopback. Packet sent in from this port is sent out from the same port. This packet is not sent to other ports.
20	R/W	1	LEARN_EN_5	Enable learn operation 0 = Does not learn new MAC address to ARL table 1 = Enable hardware learn new MAC address into ARL table.
19	RO	0	RESERVED	

Table 5-141 PORT5_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
18:16	RO	3'h4	PORT_STATE_5	Port state. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree. 000 = Disable mode. The port is completely disable, and can not receive or transmit any frames. 001 = Blocking mode. In this state, the port forwards received management frames to the designed port only. Any other frames can not be transmitted or received by the port, and without learning any SA address. 010 = Listening mode. In this state, the port receives and transmits only management frames, but without learning any SA address. Any other frames can not be transmitted or received by the port. 011 = Learning mode. In this state, the port learns all SA, and discards all frames except management frames, and only management frames allowed to be transmitted out. 100 = Forward mode. In this state, the port learns all SA, transmits and receives all frames like normal.
15	RO	0	RESERVED	
14:12	RO	0	RESERVED	
11	R/W	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_5	1 = Force to use part-based VLAN enable. If this bit is set to 1, use part-based VLAN & VLAN table result to determine destination port.
9:8	R/W	2'0	VLAN_MODE_5	802.1q mode for this port. 00 = 802.1q disable. Use part-based VLAN only. 01 = Fallback. Enable 802.1q for all received frames. Do not discard ingress membership violation and use the part-based VLAN if the frame's VID is not contained in VLAN table. 10 = Check. Enable 802.1q for all received frames. Do not discard ingress membership violation but discard frames which VID is not contained in VLAN table. 11 = Secure. Enable 802.1q for all received frames. Discard frames with ingress membership violation or whose VID is not contained in the VLAN table.
7	RO	'h6F	RESERVED	
6:0	R/W	b00	PORT_VID_MEM_5	Port-based VLAN member. Each bit restricts which port can send frames to. To send frames to port0, bit[16] must be set to 1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

5.6.37 PORT5_PRI_CTRL

Address offset: 0x06A0

Table 5-142 summarizes the port 5 priority control register.

Table 5-142 PORT5_PRI_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	RO	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_5	Enable egress MAC-based VLAN
19	RO	0	RESERVED	
18	R/W	0	DA_PRI_EN_5	DA priority selected level for QoS. There are five levels of priority for QoS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
17	R/W	0	VLAN_PRI_EN_5	DA priority selected level for QoS.
16	R/W	0	IP_PRI_EN_5	IP priority selected level for QoS.
15:8	RO	0	RESERVED	
7:6	R/W	0	DA_PRI_SEL_5	DA priority selected level for QoS. There are five levels of priority for QoS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_5	DA priority selected level for QoS.
3:2	R/W	2	IP_PRI_SEL_5	IP priority selected level for QoS.
1:0	RO	0	RESERVED	

5.6.38 PORT5_LEARN_LIMIT

Address offset: 0x06A4

Table 5-143 summarizes the port 5 learn limit control register.

Table 5-143 PORT5_LEARN_LIMIT bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_5	Drop or redirect the ingress frame to CPU when new group address coming but learned group address already reach the limitation
28	R/W	0	SA_LEARN_LIMIT_DROP_EN_5	Drop or redirect the ingress frame to CPU when new SA coming but learned SA already reach the limitation

Table 5-143 PORT5_LEARN_LIMIT bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
27	R/W	0	IGMP_LEARN_LIMIT_EN_5	1 = IGMP learn limit enable.
26:16	R/W	0	IGMP_JOIN_CNT_5	Hardware join IGMP. When join new entry or new port to IGMP + 1, leave or age - 1.
15:12	R/W	7	SA_LEARN_STATUS_5	If less than 0x7, dynamic can be fresh to setting value and age.
11	R/W	0	SA_LEARN_LIMIT_EN_5	1 = SA learn limit enable.
10:0	R/W	0	SA_LEARN_CNT_5	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: Indicate the MAC limit number is 0 1: Indicate the MAC limit number is 1 2: Indicate the MAC limit number is 2 ... and so on... until: 1024: Indicate the MAC limit is 1024

5.6.39 PORT6_LOOKUP_CTRL

Address offset: 0x06A8

Table 5-144 summarizes the port 6 lookup control register.

Table 5-144 PORT6_LOOKUP_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	MULTICAST_DROP_EN_6	1 = Drop the multicast packet from this port. Do not drop IGMP/MLD join/leave and Special DIP packet.
30:29	RO	0	RESERVED	
28	R/W	0	UNI_LEAKY_EN_6	Unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. If MAC receive unicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based and 802.1q).

Table 5-144 PORT6_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
27	R/W	0	MULTI_LEAKY_EN_6	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKY_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1, only frame with DA in ARL table and LEAKY_EN bit is set to 1 can be forward as leaky VLAN, ignore MULTI_LEAKY_EN. If MAC receive multicast frame from this port which forwards as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include part-based VLAN and 802.1q).
26	R/W	0	ARP_LEAKY_EN_6	0 = ARP frame can not cross VLAN 1 = If MAC receive ARP frame from this port, it can cross all VLAN (include part-based VLAN and 802.1q).
25	R/W	0	ING_MIRROR_EN_6	Ingress port mirror. If this bit is set to 1, all packets received from this port is copied to mirror port.
24	RO	0	RESERVED	
23	RO	0	RESERVED	
22	RO	0	RESERVED	
21	R/W	0	PORT_LOOPBACK_EN_6	0 = Normal forwarding 1 = Loop back. Packet sent in from this port is sent out from the same port. This packet is not sent to other ports.
20	R/W	1	LEARN_EN_6	Enable learn operation 0 = Do not learn new MAC address to ARL table 1 = Enable hardware learn new MAC address into ARL table
19	RO	0	RESERVED	
18:16	RO	3'h4	PORT_STATE_6	Port state. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1d Spanning Tree. 000 = Disable mode. The port is completely disable, and can not receive or transmit any frames. 001 = Blocking mode. In this state, the port forwards received management frames to the designed port only. Any other frames can not be transmitted or received by the port, and without learning any SA address. 010 = Listening mode. In this state, the port receives and transmits only management frames, but without learning any SA address. Any other frames can not be transmitted or received by the port. 011 = Learning mode. In this state, the port learns all SA, and discards all frames except management frames, and only management frames allowed to be transmitted out. 100 = Forward mode. In this state, the port learns all SA, transmits and receives all frames like normal.

Table 5-144 PORT6_LOOKUP_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
15	RO	0	RESERVED	
14:12	RO	0	RESERVED	
11	R/W	0	RESERVED	
10	R/W	0	FORCE_PORT_VLAN_EN_6	1 = Force to use part-based VLAN enable. If this bit is set to 1, use part-based VLAN & VLAN table result to determine destination port.
9:8	R/W	2'0	VLAN_MODE_6	802.1q mode for this port. 00 = 802.1q disable. Use part-based VLAN only. 01 = Fallback. Enable 802.1q for all received frames. Do not discard ingress membership violation and use the part-based VLAN if the frame's VID is not contained in VLAN table. 10 = Check. Enable 802.1q for all received frames. Do not discard ingress membership violation but discard frames which VID is not contained in VLAN table. 11 = Secure. Enable 802.1q for all received frames. Discard frames with ingress membership violation or whose VID is not contained in the VLAN table.
7	RO	'h6F	RESERVED	
6:0	R/W	b00	PORT_VID_MEM_6	Port -based VLAN member. Each bit restricts which port can send frames to. To send frames to port0, bit[16] must be set to 1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they received in.

5.6.40 PORT6_PRI_CTRL

Address offset: 0x06AC

Table 5-145 summarizes the port 6 priority control register.

Table 5-145 PORT6_PRI_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	RO	0	RESERVED	
20	R/W	0	EG_MAC_BASE_VLAN_EN_6	Enable egress MAC-based VLAN
19	RO	0	RESERVED	
18	R/W	0	DA_PRI_EN_6	DA priority selected level for QoS. There are five levels of priority for QoS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.

Table 5-145 PORT6_PRI_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
17	R/W	0	VLAN_PRI_EN_6	DA priority selected level for QoS.
16	R/W	0	IP_PRI_EN_6	IP priority selected level for QoS.
15:8	RO	0	RESERVED	
7:6	R/W	0	DA_PRI_SEL_6	DA priority selected level for QoS. There are five levels of priority for QoS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL_6	DA priority selected level for QoS.
3:2	R/W	2	IP_PRI_SEL_6	IP priority selected level for QoS.
1:0	RO	0	RESERVED	

5.6.41 PORT6_LEARN_LIMIT

Address offset: 0x06B0

Table 5-146 summarizes the port 6 learn limit control register.

Table 5-146 PORT6_LEARN_LIMIT bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29	R/W	0	IGMP_LEARN_LIMIT_DROP_EN_6	Drop or redirect the ingress frame to CPU when new group address coming but learned group address already reach the limitation
28	R/W	0	SA_LEARN_LIMIT_DROP_EN_6	Drop or redirect the ingress frame to CPU when new SA coming but learned SA already reach the limitation
27	R/W	0	IGMP_LEARN_LIMIT_EN_6	1 = IGMP learn limit enable.
26:16	R/W	0	IGMP_JOIN_CNT_6	Hardware join IGMP. When join new entry or new port to IGMP + 1, leave or age - 1.
15:12	R/W	7	SA_LEARN_STATUS_6	If less than 0x7, dynamic can be fresh to setting value and age.
11	R/W	0	SA_LEARN_LIMIT_EN_6	1 = SA learn limit enable.
10:0	R/W	0	SA_LEARN_CNT_6	The MAC address can be learned and written to the ARL table — only dynamic entry is counted 0: Indicate the MAC limit number is 0 1: Indicate the MAC limit number is 1 2: Indicate the MAC limit number is 2 ... and so on... until: 1024: Indicate the MAC limit is 1024

5.6.42 GOL_TRUNK_CTRL0

Address offset: 0x0700

Table 5-147 summarizes the global trunk control 0 register.

Table 5-147 GOL_TRUNK_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	TRUNK3_EN	Trunk 3 enable
30:24	R/W	0	TRUNK3_MEM	Trunk 3 member bitmap
23	R/W	0	TRUNK2_EN	Trunk 2 enable
22:16	R/W	0	TRUNK2_MEM	Trunk 2 member bitmap
15	R/W	0	TRUNK1_EN	Trunk 1 enable
14:8	R/W	0	TRUNK1_MEM	Trunk 1 member bitmap
7	R/W	0	TRUNK0_EN	Trunk 0 enable
6:0	R/W	0	TRUNK0_MEM	Trunk 0 member bitmap

5.6.43 GOL_TRUNK_CTRL1

Address offset: 0x0704

Table 5-148 summarizes the global trunk control 1 register.

Table 5-148 GOL_TRUNK_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	TRUNK1_MEM3_EN	Trunk 1 member 3 enable
30:28	R/W	0	TRUNK1_MEM3_NUM	Trunk 1 member 3 port number
27	R/W	0	TRUNK1_MEM2_EN	Trunk 1 member 2 enable
26:24	R/W	0	TRUNK1_MEM2_NUM	Trunk 1 member 2 port number
23	R/W	0	TRUNK1_MEM1_EN	Trunk 1 member 1 enable
22:20	R/W	0	TRUNK1_MEM1_NUM	Trunk 1 member 1 port number
19	R/W	0	TRUNK1_MEM0_EN	Trunk 1 member 0 enable
18:16	R/W	0	TRUNK1_MEM0_NUM	Trunk 1 member 0 port number
15	R/W	0	TRUNK0_MEM3_EN	Trunk 0 member 3 enable
14:12	R/W	0	TRUNK0_MEM3_NUM	Trunk 0 member 3 port number
11	R/W	0	TRUNK0_MEM2_EN	Trunk 0 member 2 enable
10:8	R/W	0	TRUNK0_MEM2_NUM	Trunk 0 member 2 port number
7	R/W	0	TRUNK0_MEM1_EN	Trunk 0 member 1 enable
6:4	R/W	0	TRUNK0_MEM1_NUM	Trunk 0 member 1 port number

Table 5-148 GOL_TRUNK_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
3	R/W	0	TRUNK0_MEM0_EN	Trunk 0 member 0 enable
2:0	R/W	0	TRUNK0_MEM0_NUM	Trunk 0 member 0 port number

5.6.44 GOL_TRUNK_CTRL2

Address offset: 0x0708

Table 5-149 summarizes the global trunk control 2 register.

Table 5-149 GOL_TRUNK_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	TRUNK3_MEM3_EN	Trunk 3 member 3 enable
30:28	R/W	0	TRUNK3_MEM3_NUM	Trunk 3 member 3 port number
27	R/W	0	TRUNK3_MEM2_EN	Trunk 3 member 2 enable
26:24	R/W	0	TRUNK3_MEM2_NUM	Trunk 3 member 2 port number
23	R/W	0	TRUNK3_MEM1_EN	Trunk 3 member 1 enable
22:20	R/W	0	TRUNK3_MEM1_NUM	Trunk 3 member 1 port number
19	R/W	0	TRUNK3_MEM0_EN	Trunk 3 member 0 enable
18:16	R/W	0	TRUNK3_MEM0_NUM	Trunk 3 member 0 port number
15	R/W	0	TRUNK2_MEM3_EN	Trunk 2 member 3 enable
14:12	R/W	0	TRUNK2_MEM3_NUM	Trunk 2 member 3 port number
11	R/W	0	TRUNK2_MEM2_EN	Trunk 2 member 2 enable
10:8	R/W	0	TRUNK2_MEM2_NUM	Trunk 2 member 2 port number
7	R/W	0	TRUNK2_MEM1_EN	Trunk 2 member 1 enable
6:4	R/W	0	TRUNK2_MEM1_NUM	Trunk 2 member 1 port number
3	R/W	0	TRUNK2_MEM0_EN	Trunk 2 member 0 enable
2:0	R/W	0	TRUNK2_MEM0_NUM	Trunk 2 member 0 port number

5.6.45 ACL_FWD_SRC_FLTR_CTRL0

Address offset: 0x0710

Table 5-150 summarizes the ACL forward source filter 0 register.

Table 5-150 ACL_FWD_SRC_FLTR_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	32'hFFFFFFFF	ACL_FWD_SRC_FLTR_CTRL0	For ACL rule [31:0] source filter control bit 0 = Disable source filter 1 = Enable source filter

5.6.46 ACL_FWD_SRC_FLTR_CTRL1

Address offset: 0x0714

Table 5-151 summarizes the ACL forward source filter 1 register.

Table 5-151 ACL_FWD_SRC_FLTR_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	32'hFFFFFFFF	ACL_FWD_SRC_FLTR_CTRL1	For ACL rule [63:32] source filter control bit 0 = Disable source filter 1 = Enable source filter

5.6.47 ACL_FWD_SRC_FLTR_CTRL2

Address offset: 0x0718

Table 5-151 summarizes the ACL forward source filter 2 register.

Table 5-152 ACL_FWD_SRC_FLTR_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	32'hFFFFFFFF	ACL_FWD_SRC_FLTR_CTRL2	For ACL rule [95:64] source filter control bit 0 = Disable source filter 1 = Enable source filter

5.7 QM register (offset range: 0x0800–0x0B70)

Table 5-153 summarizes the QM registers.

Table 5-153 QM register summary

Name	Offset range
Global flow control threshold register	0x0800
QM control register	0x0808
WAN priority to queue mapping register	0x0810

Table 5-153 QM register summary (cont.)

Name	Offset range
LAN priority to queue mapping register	0x0814
Port0 WRR control register	0x0830
Port1 WRR control register	0x0834
Port2 WRR control register	0x0838
Port3 WRR control register	0x083C
Port4 WRR control register	0x0840
Port5 WRR control register	0x0844
Port6 WRR control register	0x0848
Port0 egress rate limit control register	0x0890–0x08AC
Port1 egress rate limit control register	0x08B0–0x08CC
Port2 egress rate limit control register	0x08D0–0x08EC
Port3 egress rate limit control register	0x08F0–0x090C
Port4 egress rate limit control register	0x0910–0x092C
Port5 egress rate limit control register	0x0930–0x094C
Port6 egress rate limit control register	0x0950–0x096C
Port0 HOL control register	0x0970–0x0974
Port1 HOL control register	0x0978–0x097C
Port2 HOL control register	0x0980–0x0984
Port3 HOL control register	0x0988–0x098C
Port4 HOL control register	0x0990–0x0994
Port5 HOL control register	0x0998–0x099C
Port6 HOL control register	0x09A0–0x09A4
Port0 flow control threshold register	0x09B0
Port1 flow control threshold register	0x09B4
Port2 flow control threshold register	0x09B8
Port3 flow control threshold register	0x09BC
Port4 flow control threshold register	0x09C0
Port5 flow control threshold register	0x09C4
Port6 flow control threshold register	0x09C8
ACL policy mode register	0x09F0
ACL counter mode register	0x09F4
ACL policy counter reset register	0x09F8
ACL0 rate limit control register	0x0A00–0x0A04
ACL1 rate limit control register	0x0A08–0x0A0C
ACL2 rate limit control register	0x0A10–0x0A14
ACL3 rate limit control register	0x0A18–0x0A1C

Table 5-153 QM register summary (cont.)

Name	Offset range
ACL4 rate limit control register	0x0A20–0x0A24
ACL5 rate limit control register	0x0A28–0x0A2C
ACL6 rate limit control register	0x0A30–0x0A34
ACL7 rate limit control register	0x0A38–0x0A3C
ACL8 rate limit control register	0x0A40–0x0A44
ACL9 rate limit control register	0x0A48–0x0A4C
ACL10 rate limit control register	0x0A50–0x0A54
ACL11 rate limit control register	0x0A58–0x0A5C
ACL12 rate limit control register	0x0A60–0x0A64
ACL13 rate limit control register	0x0A68–0x0A6C
ACL14 rate limit control register	0x0A70–0x0A74
ACL15 rate limit control register	0x0A78–0x0A7C
ACL16 rate limit control register	0x0A80–0x0A84
ACL17 rate limit control register	0x0A88–0x0A8C
ACL18 rate limit control register	0x0A90–0x0A94
ACL19 rate limit control register	0x0A98–0x0A9C
ACL20 rate limit control register	0x0AA0–0x0AA4
ACL21 rate limit control register	0x0AA8–0x0AAC
ACL22 rate limit control register	0x0AB0–0x0AB4
ACL23 rate limit control register	0x0AB8–0x0ABC
ACL24 rate limit control register	0x0AC0–0x0AC4
ACL25 rate limit control register	0x0AC8–0x0ACC
ACL26 rate limit control register	0x0AD0–0x0AD4
ACL27 Rate limit control register	0x0AD8–0x0ADC
ACL28 rate limit control register	0x0AE0–0x0AE4
ACL29 rate limit control register	0x0AE8–0x0AEC
ACL30 rate limit control register	0x0AF0–0x0AF4
ACL31 rate limit control register	0x0AF8–0x0AFC
Port0 ingress rate limit control register	0x0B00–0x0B08
Port1 ingress rate limit control register	0x0B10–0x0B18
Port2 ingress rate limit control register	0x0B20–0x0B28
Port3 ingress rate limit control register	0x0B30–0x0B38
Port4 ingress rate limit control register	0x0B40–0x0B48
Port5 ingress rate limit control register	0x0B50–0x0B58
Port6 ingress rate limit control register	0x0B60–0x0B68
To CPU frame remap priority control register	0x0B70

5.7.1 GLOBAL_FLOW_THD

Address offset: 0x0800

Table 5-154 summarizes the global flow control register.

Table 5-154 GLOBAL_FLOW_THD bit description

Bits	R/W	Initial value	Mnemonic	Description
31:25	RO	0	RESERVED	
24:16	R/W	'h120	GOL_XON_THRES	Global base transmit on threshold. When block memory used by all ports less than this value, MAC sends out pause off frame, and link partner starts transmitting frame out.
15:9	RO	0	RESERVED	
8:0	R/W	'h188	GOL_XOFF_THRES	Global base transmit off threshold. When block memory used by all ports more than this value, MAC sends out pause on frame, and link partner stops transmitting frame out.

5.7.2 QM_CTRL_REG

Address offset: 0x0808

Table 5-155 summarizes the QM control register.

Table 5-155 QM_CTRL_REG bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29:28	RO	0	RESERVED	
27:26	RO	0	RESERVED	
25:23	RO	0	RESERVED	
22:16	R/W	7'h7F	GOL_FLOW_EN	Global flow control enable when global threshold is reached. Bit[16] for port0; bit[17] for port1.
15:11	RO	0	RESERVED	
10	R/W	0	QM_FUNC_TEST	1 = Function test, QM drops all packets from port1,2,3,4,5.
9	R/W	0	MS_FC_EN	Multicast server flow control enable
8	RO	0	RESERVED	
7	R/W	0	RATE_DROP_EN	Drop packet enable due to rate limit. 0 = Switch uses flow control to the source port due to rate limit; if the port does not stop, switch drops frame from that port. 1 = Switch drops frames due to rate limit.

Table 5-155 QM_CTRL_REG bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
6	R/W	0	FLOW_DROP_EN	0 = Switch does not drop packets due to flow control. 1 = Packet could be dropped due to flow control except the highest priority packet.
5:0	R/W	'hE	FLOW_DROP_CNT	Maximum free queue could be use after the port has been flow control. Then packets is drop except the highest priority. Default value 'hE is set to normal packets which length is no more than 1518 bytes. For jumbo frame, 'd33 is commanded.

5.7.3 WAN_QUEUE_MAP_REG

Address offset: 0x0810

Table 5-156 summarizes the WAN port priority to queue mapping register.

Table 5-156 WAN_QUEUE_MAP_REG bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	R/W	0	WAN_PRI_QUEUE_0X7	The destination queue for priority value 0x7 in port 0, 5 and 6
27	RO	0	RESERVED	
26:24	R/W	0	WAN_PRI_QUEUE_0X6	The destination queue for priority value 0x6 in port 0, 5 and 6
23	RO	0	RESERVED	
22:20	R/W	0	WAN_PRI_QUEUE_0X5	The destination queue for priority value 0x5 in port 0, 5 and 6
19	RO	0	RESERVED	
18:16	R/W	0	WAN_PRI_QUEUE_0X4	The destination queue for priority value 0x4 in port 0, 5 and 6
15	RO	0	RESERVED	
14:12	R/W	0	WAN_PRI_QUEUE_0X3	The destination queue for priority value 0x3 in port 0, 5 and 6
11	RO	0	RESERVED	
10:8	R/W	0	WAN_PRI_QUEUE_0X2	The destination queue for priority value 0x2 in port 0, 5 and 6
7	RO	0	RESERVED	
6:4	R/W	0	WAN_PRI_QUEUE_0X1	The destination queue for priority value 0x1 in port 0, 5 and 6

Table 5-156 WAN_QUEUE_MAP_REG bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
3	RO	0	RESERVED	
2:0	R/W	0	WAN_PRI_QUEUE_0X0	The destination queue for priority value 0x0 in port 0, 5 and 6

5.7.4 LAN_QUEUE_MAP_REG

Address offset: 0x0814

Table 5-157 summarizes the LAN port priority to queue mapping register.

Table 5-157 LAN_QUEUE_MAP_REG bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29:28	R/W	0	LAN_PRI_QUEUE_0X7	The destination queue for priority value 0x7 in port 1, 2, 3 and 4
27:26	RO	0	RESERVED	
25:24	R/W	0	LAN_PRI_QUEUE_0X6	The destination queue for priority value 0x6 in port 1, 2, 3 and 4
23:22	RO	0	RESERVED	
21:20	R/W	0	LAN_PRI_QUEUE_0X5	The destination queue for priority value 0x5 in port 1, 2, 3 and 4
19:18	RO	0	RESERVED	
17:16	R/W	0	LAN_PRI_QUEUE_0X4	The destination queue for priority value 0x4 in port 1, 2, 3 and 4
15:14	RO	0	RESERVED	
13:12	R/W	0	LAN_PRI_QUEUE_0X3	The destination queue for priority value 0x3 in port 1, 2, 3 and 4
11:10	RO	0	RESERVED	
9:8	R/W	0	LAN_PRI_QUEUE_0X2	The destination queue for priority value 0x2 in port 1, 2, 3 and 4
7:6	RO	0	RESERVED	
5:4	R/W	0	LAN_PRI_QUEUE_0X1	The destination queue for priority value 0x1 in port 1, 2, 3 and 4
3:2	RO	0	RESERVED	
1:0	R/W	0	LAN_PRI_QUEUE_0X0	The destination queue for priority value 0x0 in port 1, 2, 3 and 4

5.7.5 PORT0_WRR_CTRL

Address offset: 0x0830

Table 5-158 summarizes the port 0 WRR control register.

Table 5-158 PORT0_WRR_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	R/W	00	WEIGHT_PRI_CTRL_0	00 = Strict priority 01 = Only highest queue use strict priority; others use weighted fair queuing scheme 10 = The highest two queues use strict priority; other two queues use weighted fair queuing scheme. 11 = All queues use weighted fair queuing scheme which defined in WRR_PRI3/2/1/0.
29:25	RO	8	WRR_PRI5_1	WRR setting for priority 5
24:20	RO	8	WRR_PRI4_1	WRR setting for priority 4
19:15	R/W	8	WRR_PRI3_0	WRR setting for priority 3
14:10	R/W	4	WRR_PRI2_0	WRR setting for priority 2
9:5	R/W	2	WRR_PRI1_0	WRR setting for priority 1
4:0	R/W	1	WRR_PRI0_0	WRR setting for priority 0

5.7.6 PORT1_WRR_CTRL

Address offset: 0x0834

Table 5-159 summarizes the port 1 WRR control register.

Table 5-159 PORT1_WRR_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	R/W	00	WEIGHT_PRI_CTRL_1	00 = Strict priority 01 = Only highest queue use strict priority; others use weighted fair queuing scheme 10 = The highest two queues use strict priority; other two queues use weighted fair queuing scheme. 11 = All queues use weighted fair queuing scheme which defined in WRR_PRI3/2/1/0.
29:25	RO	8	RESERVED	
24:20	RO	8	RESERVED	
19:15	R/W	8	WRR_PRI3_1	WRR setting for priority 3
14:10	R/W	4	WRR_PRI2_1	WRR setting for priority 2
9:5	R/W	2	WRR_PRI1_1	WRR setting for priority 1
4:0	R/W	1	WRR_PRI0_1	WRR setting for priority 0

5.7.7 PORT2_WRR_CTRL

Address offset: 0x0838

Table 5-160 summarizes the port 2 WRR control register.

Table 5-160 PORT2_WRR_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	R/W	00	WEIGHT_PRI_CTRL_2	00 = Strict priority 01 = Only highest queue use strict priority; others use weighted fair queuing scheme 10 = The highest two queues use strict priority; other two queues use weighted fair queuing scheme. 11 = All Queues use weighted fair queuing scheme which defined in WRR_PRI3/2/1/0.
29:25	RO	8	RESERVED	
24:20	RO	8	RESERVED	
19:15	R/W	8	WRR_PRI3_2	WRR setting for priority 3
14:10	R/W	4	WRR_PRI2_2	WRR setting for priority 2
9:5	R/W	2	WRR_PRI1_2	WRR setting for priority 1
4:0	R/W	1	WRR_PRI0_2	WRR setting for priority 0

5.7.8 PORT3_WRR_CTRL

Address offset: 0x083C

Table 5-161 summarizes the port 3 WRR control register.

Table 5-161 PORT3_WRR_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	R/W	00	WEIGHT_PRI_CTRL_3	00 = Strict priority 01 = Only highest queue use strict priority; others use weighted fair queuing scheme 10 = The highest two queues use strict priority, other two queues use weighted fair queuing scheme. 11 = All queues use weighted fair queuing scheme which defined in WRR_PRI3/2/1/0.
29:25	R/W	8	RESERVED	
24:20	R/W	8	RESERVED	
19:15	R/W	8	WRR_PRI3_3	WRR setting for priority 3
14:10	R/W	4	WRR_PRI2_3	WRR setting for priority 2

Table 5-161 PORT3_WRR_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
9:5	R/W	2	WRR_PRI1_3	WRR setting for priority 1
4:0	R/W	1	WRR_PRI0_3	WRR setting for priority 0

5.7.9 PORT4_WRR_CTRL

Address offset: 0x0840

Table 5-162 summarizes the port 4 WRR control register.

Table 5-162 PORT4_WRR_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	R/W	00	WEIGHT_PRI_CTRL_4	00 = Strict priority 01 = Only highest queue use strict priority; others use weighted fair queuing scheme. 10 = The highest two queues use strict priority, other two queues use weighted fair queuing scheme. 11 = All queues use weighted fair queuing scheme which defined in WRR_PRI3/2/1/0.
29:25	RO	8	RESERVED	
24:20	RO	8	RESERVED	
19:15	R/W	8	WRR_PRI3_4	WRR setting for priority 3
14:10	R/W	4	WRR_PRI2_4	WRR setting for priority 2
9:5	R/W	2	WRR_PRI1_4	WRR setting for priority 1
4:0	R/W	1	WRR_PRI0_4	WRR setting for priority 0

5.7.10 PORT5_WRR_CTRL

Address offset: 0x0844

Table 5-163 summarizes the port 5 WRR control register.

Table 5-163 PORT5_WRR_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	R/W	00	WEIGHT_PRI_CTRL_5	00 = Strict priority 01 = Only highest queue use strict priority; others use weighted fair queuing scheme 10 = The highest two queues use strict priority, other two queues use weighted fair queuing scheme. 11 = All queues use weighted fair queuing scheme which defined in WRR_PRI3/2/1/0.
29:25	R/W	8	WRR_PRI5_5	WRR setting for priority 5
24:20	R/W	8	WRR_PRI4_5	WRR setting for priority 4
19:15	R/W	8	WRR_PRI3_5	WRR setting for priority 3
14:10	R/W	4	WRR_PRI2_5	WRR setting for priority 2
9:5	R/W	2	WRR_PRI1_5	WRR setting for priority 1
4:0	R/W	1	WRR_PRI0_5	WRR setting for priority 0

5.7.11 PORT6_WRR_CTRL

Address offset: 0x0848

Table 5-164 summarizes the port 6 WRR control register.

Table 5-164 PORT6_WRR_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	R/W	00	WEIGHT_PRI_CTRL_6	00 = Strict priority 01 = Only highest queue use strict priority; others use weighted fair queuing scheme 10 = The highest two queues use strict priority, other two queues use weighted fair queuing scheme. 11 = All Queues use weighted fair queuing scheme which defined in WRR_PRI3/2/1/0.
29:25	R/W	8	WRR_PRI5_6	WRR setting for priority 5
24:20	R/W	8	WRR_PRI4_6	WRR setting for priority 4
19:15	R/W	8	WRR_PRI3_6	WRR setting for priority 3
14:10	R/W	4	WRR_PRI2_6	WRR setting for priority 2
9:5	R/W	2	WRR_PRI1_6	WRR setting for priority 1
4:0	R/W	1	WRR_PRI0_6	WRR setting for priority 0

5.7.12 PORT0_EG_RATE_CTRL0

Address offset: 0x0890

Table 5-165 summarizes the port 0 rate limit control 0 register.

Table 5-165 PORT0_EG_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_0	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from port 0.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_0	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from port 0.

5.7.13 PORT0_EG_RATE_CTRL1

Address offset: 0x0894

Table 5-166 summarizes the port 0 rate limit control 1 register.

Table 5-166 PORT0_EG_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_0	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from port 0.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_0	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from port 0.

5.7.14 PORT0_EG_RATE_CTRL2

Address offset: 0x0898

Table 5-167 summarizes the port 0 rate limit control 2 register.

Table 5-167 PORT0_EG_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_CIR_0	Egress rate limit for priority 5. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. If these bits are set to 15'h0, no priority 5 frame is send out from port 0.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_CIR_0	Egress rate limit for priority 4. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. If these bits are set to 15'h0, no priority 4 frame is send out from port 0.

5.7.15 PORT0_EG_RATE_CTRL3

Address offset: 0x089C

Table 5-168 summarizes the port 0 rate limit control 3 register.

Table 5-168 PORT0_EG_RATE_CTRL3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_0	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_0	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.16 PORT0_EG_RATE_CTRL4

Address offset: 0x08A0

Table 5-169 summarizes the port 0 rate limit control 4 register.

Table 5-169 PORT0_EG_RATE_CTRL4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_0	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR_0	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.17 PORT0_EG_RATE_CTRL5

Address offset: 0x08A4

Table 5-170 summarizes the port 0 rate limit control 5 register.

Table 5-170 PORT0_EG_RATE_CTRL5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_EIR_0	Egress rate limit for priority 5. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. If these bits are set to 15'h0, no priority 5 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_EIR_0	Egress rate limit for priority 4. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. If these bits are set to 15'h0, no priority 4 frame is send out from this port.

5.7.18 PORT0_EG_RATE_CTRL6

Address offset: 0x08A8

Table 5-171 summarizes the port 0 rate limit control 6 register.

Table 5-171 PORT0_EG_RATE_CTRL6 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_0	Committed burst size for priority 3 Commit burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
27	RO	0	RESERVED	

Table 5-171 PORT0_EG_RATE_CTRL6 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
26:24	R/W	0	EG_PRI3_EBS_0	Excess burst size for priority 3 Excess burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
23	RO	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_0	Committed burst size for priority 2 Commit burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
19	RO	0	RESERVED	

Table 5-171 PORT0_EG_RATE_CTRL6 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
18:16	R/W	0	EG_PRI2_EBS_0	Excess burst size for priority 2 Excess burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
15	RO	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_0	Committed burst size for priority 1 Commit burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
11	RO	0	RESERVED	

Table 5-171 PORT0_EG_RATE_CTRL6 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
10:8	R/W	0	EG_PRI1_EBS_0	Excess burst size for priority 1 Excess burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
7	RO	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_0	Committed burst size for priority 0 Commit burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets

Table 5-171 PORT0_EG_RATE_CTRL6 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
3	RO	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_0	Excess burst size for priority 0 Excess burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets

5.7.19 PORT0_EG_RATE_CTRL7

Address offset: 0x08AC

[Table 5-172](#) summarizes the port0 rate limit control 7 register.

Table 5-172 PORT0_EG_RATE_CTRL7 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	R/W	0	EG_PRI5_CBS_0	Committed burst size for priority 5 Commit burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
27	RO	0	RESERVED	
26:24	R/W	0	EG_PRI5_EBS_0	Excess burst size for priority 5 Excess burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
23	RO	0	RESERVED	

Table 5-172 PORT0_EG_RATE_CTRL7 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
22:20	R/W	0	EG_PRI4_CBS_0	Committed burst size for priority 4 Commit burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
19	RO	0	RESERVED	
18:16	R/W	0	EG_PRI4_EBS_0	Excess burst size for priority 4 Excess burst size: 0: 0k bytes 1: 2k bytes 2: 4k bytes 3: 8k bytes 4: 16k bytes 5: 32k bytes 6: 128k bytes 7: 512k bytes For packet mode: 0: 0k packets 1: 2k packets 2: 4k packets 3: 16k packets 4: 64k packets 5: 256k packets 6: 512k packets 7: 1024k packets
15:14	RO	0	RESERVED	
13	R/W	0	EG_PRI5_RATE_UNIT_0	Rate limit unit for queue 5: 0 = Bytes 1 = Packets

Table 5-172 PORT0_EG_RATE_CTRL7 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
12	R/W	0	EG_PRI4_RATE_UNIT_0	Rate limit unit for queue 4: 0 = Bytes 1 = Packets
11	R/W	0	EG_PRI3_RATE_UNIT_0	Rate limit unit for queue 3: 0 = Bytes 1 = Packets
10	R/W	0	EG_PRI2_RATE_UNIT_0	Rate limit unit for queue 2: 0 = Bytes 1 = Packets
9	R/W	0	EG_PRI1_RATE_UNIT_0	Rate limit unit for queue 1: 0 = Bytes 1 = Packets
8	R/W	0	EG_PRI0_RATE_UNIT_0	Rate limit unit for queue 0: 0 = Bytes 1 = Packets
7:5	RO	0	RESERVED	
4	R/W	0	EGRESS_MANAGE_RATE_EN_0	Enable management frame to be calculate to egress rate limit.
3	R/W	0	EGRESS_RATE_EN_0	Enable part-based rate limit. Rate is set at EG_PRI0_CIR Enable port-based maximum burst size. Max burst size is set at EG_PRI0_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_0	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

5.7.20 PORT1_EG_RATE_CTRL0

Address offset: 0x08B0

Table 5-173 summarizes the port 1 rate limit control 0 register.

Table 5-173 PORT1_EG_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_1	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_1	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.21 PORT1_EG_RATE_CTRL1

Address offset: 0x08B4

Table 5-174 summarizes the port 1 rate limit control 1 register.

Table 5-174 PORT1_EG_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_1	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_1	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.22 PORT1_EG_RATE_CTRL2

Address offset: 0x08BC

Table 5-175 summarizes the port 1 rate limit control 2 register.

Table 5-175 PORT1_EG_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_1	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_1	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.23 PORT1_EG_RATE_CTRL3

Address offset: 0x08C0

Table 5-176 summarizes the port1 rate limit control 3 register.

Table 5-176 PORT1_EG_RATE_CTRL3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_1	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR_1	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.24 PORT1_EG_RATE_CTRL4

Address offset: 0x08C8

Table 5-177 summarizes the port 1 rate limit control 4 register.

Table 5-177 PORT1_EG_RATE_CTRL4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_1	Committed burst size for priority 3
27	RO	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_1	Excess burst size for priority 3
23	RO	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_1	Committed burst size for priority 2
19	RO	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_1	Excess burst size for priority 2
15	RO	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_1	Committed burst size for priority 1
11	RO	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_1	Excess burst size for priority 1
7	RO	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_1	Committed burst size for priority 0
3	RO	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_1	Excess burst size for priority 0

5.7.25 PORT1_EG_RATE_CTRL5

Address offset: 0x08CC

Table 5-178 summarizes the port 1 rate limit control 5 register.

Table 5-178 PORT1_EG_RATE_CTRL5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:12	RO	0	RESERVED	
11	R/W	0	EG_PRI3_RATE_UNIT_1	Rate limit unit for queue 3: 0 = Bytes 1 = Packets
10	R/W	0	EG_PRI2_RATE_UNIT_1	Rate limit unit for queue 2: 0 = Bytes 1 = Packets
9	R/W	0	EG_PRI1_RATE_UNIT_1	Rate limit unit for queue 1: 0 = Bytes 1 = Packets

Table 5-178 PORT1_EG_RATE_CTRL5 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
8	R/W	0	EG_PRI0_RATE_UNIT_1	Rate limit unit for queue 0: 0 = Bytes 1 = Packets
7:5	RO	0	RESERVED	
4	R/W	0	EGRESS_MANAGE_RATE_EN_1	Enable management frame to be calculate to egress rate limit.
3	R/W	0	EGRESS_RATE_EN_1	Enable port-based rate limit. Rate is set at EG_PRI0_CIR Enable port-based maximum burst size also. Max burst size is set at EG_PRI0_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_1	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

5.7.26 PORT2_EG_RATE_CTRL0

Address offset: 0x08D0

Table 5-179 summarizes the port 2 rate limit control 0 register.

Table 5-179 PORT2_EG_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_2	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_2	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.27 PORT2_EG_RATE_CTRL1

Address offset: 0x08D4

Table 5-180 summarizes the port 2 rate limit control 1 register.

Table 5-180 PORT2_EG_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_2	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_2	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.28 PORT2_EG_RATE_CTRL2

Address offset: 0x08DC

Table 5-181 summarizes the port 2 rate limit control 2 register.

Table 5-181 PORT2_EG_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_2	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_2	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.29 PORT2_EG_RATE_CTRL3

Address offset: 0x08E0

Table 5-182 summarizes the port 2 rate limit control 3 register.

Table 5-182 PORT2_EG_RATE_CTRL3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_2	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR_2	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.30 PORT2_EG_RATE_CTRL4

Address offset: 0x08E8

Table 5-183 summarizes the port 2 rate limit control 4 register.

Table 5-183 PORT2_EG_RATE_CTRL4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_2	Committed burst size for priority 3
27	RO	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_2	Excess burst size for priority 3
23	RO	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_2	Committed burst size for priority 2
19	RO	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_2	Excess burst size for priority 2
15	RO	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_2	Committed burst size for priority 1
11	RO	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_2	Excess burst size for priority 1

Table 5-183 PORT2_EG_RATE_CTRL4 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
7	RO	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_2	Committed burst size for priority 0
3	RO	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_2	Excess burst size for priority 0

5.7.31 PORT2_EG_RATE_CTRL5

Address offset: 0x08EC

Table 5-184 summarizes the port 2 rate limit control 5 register.

Table 5-184 PORT2_EG_RATE_CTRL5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:12	RO	0	RESERVED	
11	R/W	0	EG_PRI3_RATE_UNIT_2	Rate limit unit for queue 3: 0 = Bytes 1 = Packets
10	R/W	0	EG_PRI2_RATE_UNIT_2	Rate limit unit for queue 2: 0 = Bytes 1 = Packets
9	R/W	0	EG_PRI1_RATE_UNIT_2	Rate limit unit for queue 1: 0 = Bytes 1 = Packets
8	R/W	0	EG_PRI0_RATE_UNIT_2	Rate limit unit for queue 0: 0 = Bytes 1 = Packets
7:5	RO	0	RESERVED	
4	R/W	0	EGRESS_MANAGE_RATE_EN_2	Enable management frame to be calculate to egress rate limit.

Table 5-184 PORT2_EG_RATE_CTRL5 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
3	R/W	0	EGRESS_RATE_EN_2	Enable port-based rate limit. Rate is set at EG_Prio_CIR Maximum burst size is also set at EG_Prio_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_2	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

5.7.32 PORT3_EG_RATE_CTRL0

Address offset: 0x08F0

Table 5-185 summarizes the port 3 rate limit control 0 register.

Table 5-185 PORT3_EG_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_3	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_3	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.33 PORT3_EG_RATE_CTRL1

Address offset: 0x08F4

Table 5-186 summarizes the port 3 rate limit control 1 register.

Table 5-186 PORT3_EG_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_3	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_3	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.34 PORT3_EG_RATE_CTRL2

Address offset: 0x08FC

[Table 5-187](#) summarizes the port 3 rate limit control 2 register.

Table 5-187 PORT3_EG_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_3	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_3	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.35 PORT3_EG_RATE_CTRL3

Address offset: 0x0900

[Table 5-188](#) summarizes the port 3 rate limit control 3 register.

Table 5-188 PORT3_EG_RATE_CTRL3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_3	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR_3	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.36 PORT3_EG_RATE_CTRL4

Address offset: 0x0908

Table 5-189 summarizes the port 3 rate limit control 4 register.

Table 5-189 PORT3_EG_RATE_CTRL4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_3	Committed burst size for priority 3
27	RO	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_3	Excess burst size for priority 3
23	RO	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_3	Committed burst size for priority 2
19	RO	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_3	Excess burst size for priority 2
15	RO	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_3	Committed burst size for priority 1
11	RO	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_3	Excess burst size for priority 1
7	RO	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_3	Committed burst size for priority 0
3	RO	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_3	Excess burst size for priority 0

5.7.37 PORT3_EG_RATE_CTRL5

Address offset: 0x090C

Table 5-190 summarizes the port 3 rate limit control 5 register.

Table 5-190 PORT3_EG_RATE_CTRL5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:12	RO	0	RESERVED	
11	R/W	0	EG_PRI3_RATE_UNIT_3	Rate limit unit for queue 3: 0 = Bytes 1 = Packets
10	R/W	0	EG_PRI2_RATE_UNIT_3	Rate limit unit for queue 2: 0 = Bytes 1 = Packets
9	R/W	0	EG_PRI1_RATE_UNIT_3	Rate limit unit for queue 1: 0 = Bytes 1 = Packets
8	R/W	0	EG_PRI0_RATE_UNIT_3	Rate limit unit for queue 0: 0 = Bytes 1 = Packets
7:5	RO	0	RESERVED	
4	R/W	0	EGRESS_MANAGE_RATE_EN_3	Enable management frame to be calculate to egress rate limit.
3	R/W	0	EGRESS_RATE_EN_3	Enable port-based rate limit. Rate is set at EG_PRI0_CIR Enable Max burst size also. Max burst size is set at EG_PRI0_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_3	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

5.7.38 PORT4_EG_RATE_CTRL0

Address offset: 0x0910

Table 5-191 summarizes the port 4 rate limit control 0 register.

Table 5-191 PORT4_EG_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_4	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_4	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.39 PORT4_EG_RATE_CTRL1

Address offset: 0x0914

Table 5-192 summarizes the port 4 rate limit control 1 register.

Table 5-192 PORT4_EG_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_4	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_4	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.40 PORT4_EG_RATE_CTRL2

Address offset: 0x091C

Table 5-193 summarizes the port 4 rate limit control 2 register.

Table 5-193 PORT4_EG_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_4	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_4	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.41 PORT4_EG_RATE_CTRL3

Address offset: 0x0920

Table 5-194 summarizes the port 4 rate limit control 3 register.

Table 5-194 PORT4_EG_RATE_CTRL3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_4	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR_4	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.42 PORT4_EG_RATE_CTRL4

Address offset: 0x0928

Table 5-195 summarizes the port 4 rate limit control 4 register.

Table 5-195 PORT4_EG_RATE_CTRL4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_4	Committed burst size for priority 3
27	RO	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_4	Excess burst size for priority 3
23	RO	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_4	Committed burst size for priority 2
19	RO	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_4	Excess burst size for priority 2
15	RO	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_4	Committed burst size for priority 1
11	RO	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_4	Excess burst size for priority 1
7	RO	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_4	Committed burst size for priority 0
3	RO	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_4	Excess burst size for priority 0

5.7.43 PORT4_EG_RATE_CTRL5

Address offset: 0x092C

Table 5-196 summarizes the port 4 rate limit control 5 register.

Table 5-196 PORT4_EG_RATE_CTRL5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	RO	0	RESERVED	
11	R/W	0	EG_PRI3_RATE_UNIT_4	Rate limit unit for queue 3: 0 = Bytes 1 = Packets
10	R/W	0	EG_PRI2_RATE_UNIT_4	Rate limit unit for queue 2: 0 = Bytes 1 = Packets
9	R/W	0	EG_PRI1_RATE_UNIT_4	Rate limit unit for queue 1: 0 = Bytes 1 = Packets

Table 5-196 PORT4_EG_RATE_CTRL5 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
8	R/W	0	EG_PRI0_RATE_UNIT_4	Rate limit unit for queue 0: 0 = Bytes 1 = Packets
7:5	RO	0	RESERVED	
4	R/W	0	EGRESS_MANAGE_RATE_EN_4	Enable management frame to be calculate to egress rate limit.
3	R/W	0	EGRESS_RATE_EN_4	Enable port-based rate limit. Rate is set at EG_PRI0_CBS Enable Max burst size also. Max burst size is set at EG_PRI0_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_4	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

5.7.44 PORT5_EG_RATE_CTRL0

Address offset: 0x0930

Table 5-197 summarizes the port 5 rate limit control 0 register.

Table 5-197 PORT5_EG_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_5	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_5	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.45 PORT5_EG_RATE_CTRL1

Address offset: 0x0934

Table 5-198 summarizes the port 5 rate limit control 1 register.

Table 5-198 PORT5_EG_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_5	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_5	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.46 PORT5_EG_RATE_CTRL2

Address offset: 0x0938

Table 5-199 summarizes the port 5 rate limit control 2 register.

Table 5-199 PORT5_EG_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_CIR_5	Egress rate limit for priority 5. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. If these bits are set to 15'h0, no priority 5 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_CIR_5	Egress rate limit for priority 4. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. If these bits are set to 15'h0, no priority 4 frame is send out from this port.

5.7.47 PORT5_EG_RATE_CTRL3

Address offset: 0x093C

Table 5-200 summarizes the port 5 rate limit control 3 register.

Table 5-200 PORT5_EG_RATE_CTRL3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_5	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_5	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.48 PORT5_EG_RATE_CTRL4

Address offset: 0x0940

Table 5-201 summarizes the port 5 rate limit control 4 register.

Table 5-201 PORT5_EG_RATE_CTRL4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_5	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR_5	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.49 PORT5_EG_RATE_CTRL5

Address offset: 0x0944

Table 5-202 summarizes the port 5 rate limit control 5 register.

Table 5-202 PORT5_EG_RATE_CTRL5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_EIR_5	Egress rate limit for priority 5. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. If these bits are set to 15'h0, no priority 5 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_EIR_5	Egress rate limit for priority 4 Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. If these bits are set to 15'h0, no priority 4 frame is send out from this port.

5.7.50 PORT5_EG_RATE_CTRL6

Address offset: 0x0948

Table 5-203 summarizes the port 5 rate limit control 6 register.

Table 5-203 PORT5_EG_RATE_CTRL6 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_5	Committed burst size for priority 3
27	RO	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_5	Excess burst size for priority 3
23	RO	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_5	Committed burst size for priority 2
19	RO	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_5	Excess burst size for priority 2
15	RO	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_5	Committed burst size for priority 1
11	RO	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_5	Excess burst size for priority 1

Table 5-203 PORT5_EG_RATE_CTRL6 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
7	RO	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_5	Committed burst size for priority 0
3	RO	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_5	Excess burst size for priority 0

5.7.51 PORT5_EG_RATE_CTRL7

Address offset: 0x094C

Table 5-204 summarizes the port 5 rate limit control 7 register.

Table 5-204 PORT5_EG_RATE_CTRL7 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	R/W	0	EG_PRI5_CBS_5	Committed burst size for priority 5
27	RO	0	RESERVED	
26:24	R/W	0	EG_PRI5_EBS_5	Excess burst size for priority 5
23	RO	0	RESERVED	
22:20	R/W	0	EG_PRI4_CBS_5	Committed burst size for priority 4
19	RO	0	RESERVED	
18:16	R/W	0	EG_PRI4_EBS_5	Excess burst size for priority 4
15:14	RO	0	RESERVED	
13	R/W	0	EG_PRI5_RATE_UNIT_5	Rate limit unit for queue 5: 0 = Bytes 1 = Packets
12	R/W	0	EG_PRI4_RATE_UNIT_5	Rate limit unit for queue 4: 0 = Bytes 1 = Packets
11	R/W	0	EG_PRI3_RATE_UNIT_5	Rate limit unit for queue 3: 0 = Bytes 1 = Packets
10	R/W	0	EG_PRI2_RATE_UNIT_5	Rate limit unit for queue 2: 0 = Bytes 1 = Packets
9	R/W	0	EG_PRI1_RATE_UNIT_5	Rate limit unit for queue 1: 0 = Bytes 1 = Packets

Table 5-204 PORT5_EG_RATE_CTRL7 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
8	R/W	0	EG_PRI0_RATE_UNIT_5	Rate limit unit for queue 0: 0 = Bytes 1 = Packets
7:5	RO	0	RESERVED	
4	R/W	0	EGRESS_MANAGE_RATE_EN_5	Enable management frame to be calculate to egress rate limit.
3	R/W	0	EGRESS_RATE_EN_5	Enable port-based rate limit. Rate is set at EG_PRI0_CIR Enable maximum burst size. Maximum burst size is set at EG_PRI0_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_5	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

5.7.52 PORT6_EG_RATE_CTRL0

Address offset: 0x0950

Table 5-205 summarizes the port 6 rate limit control 0 register.

Table 5-205 PORT6_EG_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_CIR_6	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_CIR_6	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.53 PORT6_EG_RATE_CTRL1

Address offset: 0x0954

Table 5-206 summarizes the port 6 rate limit control 1 register.

Table 5-206 PORT6_EG_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_CIR_6	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_CIR_6	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.54 PORT6_EG_RATE_CTRL2

Address offset: 0x0958

Table 5-207 summarizes the port 6 rate limit control 2 register.

Table 5-207 PORT6_EG_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_CIR_6	Egress rate limit for priority 5. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. If these bits are set to 15'h0, no priority 5 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_CIR_6	Egress rate limit for priority 4. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. If these bits are set to 15'h0, no priority 4 frame is send out from this port.

5.7.55 PORT6_EG_RATE_CTRL3

Address offset: 0x095C

Table 5-208 summarizes the port 6 rate limit control 3 register.

Table 5-208 PORT6_EG_RATE_CTRL3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI1_EIR_6	Egress rate limit for priority 1. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 1. If these bits are set to 15'h0, no priority 1 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI0_EIR_6	Egress rate limit for priority 0. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 0. If these bits are set to 15'h0, no priority 0 frame is send out from this port.

5.7.56 PORT6_EG_RATE_CTRL4

Address offset: 0x0960

Table 5-209 summarizes the port 6 rate limit control 4 register.

Table 5-209 PORT6_EG_RATE_CTRL4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI3_EIR_6	Egress rate limit for priority 3. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 3. If these bits are set to 15'h0, no priority 3 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI2_EIR_6	Egress rate limit for priority 2. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no priority 2 frame is send out from this port.

5.7.57 PORT6_EG_RATE_CTRL5

Address offset: 0x0964

Table 5-210 summarizes the port 6 rate limit control 5 register.

Table 5-210 PORT6_EG_RATE_CTRL5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:16	R/W	0x7FFF	EG_PRI5_EIR_6	Egress rate limit for priority 5. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 5. If these bits are set to 15'h0, no priority 5 frame is send out from this port.
15	RO	0	RESERVED	
14:0	R/W	0x7FFF	EG_PRI4_EIR_6	Egress rate limit for priority 4. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 4. If these bits are set to 15'h0, no priority 4 frame is send out from this port.

5.7.58 PORT6_EG_RATE_CTRL6

Address offset: 0x0968

Table 5-211 summarizes the port 6 rate limit control 6 register.

Table 5-211 PORT6_EG_RATE_CTRL6 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	R/W	0	EG_PRI3_CBS_6	Committed burst size for priority 3
27	RO	0	RESERVED	
26:24	R/W	0	EG_PRI3_EBS_6	Excess burst size for priority 3
23	RO	0	RESERVED	
22:20	R/W	0	EG_PRI2_CBS_6	Committed burst size for priority 2
19	RO	0	RESERVED	
18:16	R/W	0	EG_PRI2_EBS_6	Excess burst size for priority 2
15	RO	0	RESERVED	
14:12	R/W	0	EG_PRI1_CBS_6	Committed burst size for priority 1
11	RO	0	RESERVED	
10:8	R/W	0	EG_PRI1_EBS_6	Excess burst size for priority 1

Table 5-211 PORT6_EG_RATE_CTRL6 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
7	RO	0	RESERVED	
6:4	R/W	0	EG_PRI0_CBS_6	Committed burst size for priority 0
3	RO	0	RESERVED	
2:0	R/W	0	EG_PRI0_EBS_6	Excess burst size for priority 0

5.7.59 PORT6_EG_RATE_CTRL7

Address offset: 0x096C

Table 5-212 summarizes the port 6 rate limit control 7 register.

Table 5-212 PORT6_EG_RATE_CTRL7 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	RO	0	RESERVED	
30:28	R/W	0	EG_PRI5_CBS_6	Committed burst size for priority 5
27	RO	0	RESERVED	
26:24	R/W	0	EG_PRI5_EBS_6	Excess burst size for priority 5
23	RO	0	RESERVED	
22:20	R/W	0	EG_PRI4_CBS_6	Committed burst size for priority 4
19	RO	0	RESERVED	
18:16	R/W	0	EG_PRI4_EBS_6	Excess burst size for priority 4
15:14	RO	0	RESERVED	
13	R/W	0	EG_PRI5_RATE_UNIT_6	Rate limit unit for queue 5: 0 = Bytes 1 = Packets
12	R/W	0	EG_PRI4_RATE_UNIT_6	Rate limit unit for queue 4: 0 = Bytes 1 = Packets
11	RO	0	EG_PRI3_RATE_UNIT_6	Rate limit unit for queue 3: 0 = Bytes 1 = Packets
10	R/W	0	EG_PRI2_RATE_UNIT_6	Rate limit unit for queue 2: 0 = Bytes 1 = Packets
9	R/W	0	EG_PRI1_RATE_UNIT_6	Rate limit unit for queue 1: 0 = Bytes 1 = Packets

Table 5-212 PORT6_EG_RATE_CTRL7 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
8	R/W	0	EG_PRI0_RATE_UNIT_6	Rate limit unit for queue 0: 0 = Bytes 1 = Packets
7:5	RO	0	RESERVED	
4	R/W	0	EGRESS_MANAGE_RATE_EN_6	Enable management frame to be calculate to egress rate limit.
3	RO	0	EGRESS_RATE_EN_6	Enable Port-based rate limit. Rate is set at EG_PRI0_CIR Enable Port-based Max burst size also. Max burst size is set at EG_PRI0_CBS
2:0	R/W	3'h2	EG_TIME_SLOT_6	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

5.7.60 PORT0_HOL_CTRL0

Address offset: 0x0970

Table 5-213 summarizes the port 0 HOL control 0 register.

Table 5-213 PORT0_HOL_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_0	Most buffer can be used for this port. Buffer number is times of 8. 6'h0: 0 6'h1: No more than 8 6'h2: No more than 16 6'h3F: No more than 504
23:20	R/W	0x8	EG_PRI5_QUEUE_NUM_0	See bits[3:0]. This is for priority queue 5.
19:16	R/W	0x8	EG_PRI4_QUEUE_NUM_0	See bits[3:0]. This is for priority queue 4.
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_0	See bits[3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_0	See bits[3:0]. This is for priority queue 2.

Table 5-213 PORT0_HOL_CTRL0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_0	See bits[3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_0	Most buffer can be used for priority 0 queue. Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.61 PORT0_HOL_CTRL1

Address offset: 0x0974

Table 5-214 summarizes the port 0 HOL control 1 register.

Table 5-214 PORT0_HOL_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:17	RO	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_0	Egress port mirror. If this bit is set to 1, all packets send out through this port is copied to mirror port.
15:9	RO	0	RESERVED	
8	R/W	1	PORT_RED_EN_0	WRED enable
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_0	1 = Enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_0	1 = Enable use PRI*_QUEUE_NUM to control queue depth in this port.
5:4	RO	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_0	Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.62 PORT1_HOL_CTRL0

Address offset: 0x0978

Table 5-215 summarizes the port 1 HOL control 0 register.

Table 5-215 PORT1_HOL_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_1	Most buffer can be used for this port. Buffer number is times of 8. 6'h0: 0 6'h1: No more than 8 6'h2: No more than 16 6'h3F: No more than 504
23:20	R/W	0	RESERVED	
19:16	R/W	0	RESERVED	
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_1	See bits[3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_1	See bits[3:0]. This is for priority queue 2.
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_1	See bits[3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_1	Most buffer can be used for priority 0 queue. Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.63 PORT1_HOL_CTRL1

Address offset: 0x097C

Table 5-216 summarizes the port 1 HOL control 1 register.

Table 5-216 PORT1_HOL_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:17	RO	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_1	Egress port mirror. If this bit is set to 1, all packets send out through this port are copied to mirror port.
15:9	RO	0	RESERVED	
8	R/W	1	PORT_RED_EN_1	WRED enable
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_1	1 = Enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_1	1 = Enable use PRI*_QUEUE_NUM to control queue depth in this port.

Table 5-216 PORT1_HOL_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
5:4	RO	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_1	Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.64 PORT2_HOL_CTRL0

Address offset: 0x0980

Table 5-217 summarizes the port 2 HOL control 0 register.

Table 5-217 PORT2_HOL_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_2	Most buffer can be used for this port. Buffer number is times of 8. 6'h0: 0 6'h1: No more than 8 6'h2: No more than 16 6'h3F: No more than 504
23:20	R/W	0x8	RESERVED	
19:16	R/W	0x8	RESERVED	
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_2	See bits[3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_2	See bits[3:0]. This is for priority queue 2.
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_2	See bits[3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_2	Most buffer can be used for priority 0 queue. Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.65 PORT2_HOL_CTRL1

Address offset: 0x0984

Table 5-218 summarizes the port 2 HOL control 1 register.

Table 5-218 PORT2_HOL_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:17	RO	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_2	Egress port mirror. If this bit is set to 1, all packets send out through this port are copied to mirror port.
15:9	RO	0	RESERVED	
8	R/W	1	PORT_RED_EN_1	WRED enable
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_2	1 = Enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_2	1 = Enable use PRI*_QUEUE_NUM to control queue depth in this port.
5:4	RO	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_2	Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.66 PORT3_HOL_CTRL0

Address offset: 0x0988

Table 5-219 summarizes the port 3 HOL control 0 register.

Table 5-219 PORT3_HOL_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_3	Most buffer can be used for this port. Buffer number is times of 8. 6'h0: 0 6'h1: No more than 8 6'h2: No more than 16 6'h1F: No more than 504
23:20	R/W	0x8	RESERVED	

Table 5-219 PORT3_HOL_CTRL0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
19:16	R/W	0x8	RESERVED	
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_3	See bits[3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_3	See bits[3:0]. This is for priority queue 2.
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_3	See bits[3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_3	Most buffer can be used for priority 0 queue. Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.67 PORT3_HOL_CTRL1

Address offset: 0x098c

Table 5-220 summarizes the port 3 HOL control 1 register.

Table 5-220 PORT3_HOL_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:17	RO	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_3	Egress port mirror. If this bit is set to 1, all packets send out through this port are copied to mirror port.
15:9	RO	0	RESERVED	
8	R/W	1	PORT_RED_EN_1	WRED enable
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_3	1 = Enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_3	1 = Enable use PRI*_QUEUE_NUM to control queue depth in this port.
5:4	RO	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_3	Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.68 PORT4_HOL_CTRL0

Address offset: 0x0990

Table 5-221 summarizes the port 4 HOL control 0 register.

Table 5-221 PORT4_HOL_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_4	Most buffer can be used for this port. Buffer number is times of 8. 6'h0: 0 6'h1: No more than 8 6'h2: No more than 16 6'h3F: No more than 504
23:20	R/W	0x8	RESERVED	
19:16	R/W	0x8	RESERVED	
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_4	See bits[3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_4	See bits[3:0]. This is for priority queue 2.
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_4	See bits[3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_4	Most buffer can be used for priority 0 queue. Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.69 PORT4_HOL_CTRL1

Address offset: 0x0994

Table 5-202 summarizes the port 4 HOL control 0 register.

Table 5-222 PORT4_HOL_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:17	RO	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_4	Egress port mirror. If this bit is set to 1, all packets send out through this port are copied to mirror port.
15:9	RO	0	RESERVED	

Table 5-222 PORT4_HOL_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
8	R/W	1	PORT_RED_EN_1	WRED enable
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_4	1 = Enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_4	1 = Enable use PRI*_QUEUE_NUM to control queue depth in this port.
5:4	RO	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_4	Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.70 PORT5_HOL_CTRL0

Address offset: 0x0998

Table 5-223 summarizes the port 5 HOL control 0 register.

Table 5-223 PORT5_HOL_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_5	Most buffer can be used for this port. Buffer number is times of 8. 6'h0: 0 6'h1: No more than 8 6'h2: No more than 16 6'h3F: No more than 504
23:20	R/W	0x8	EG_PRI5_QUEUE_NUM_5	See bits[3:0]. This is for priority queue 5.
19:16	R/W	0x8	EG_PRI4_QUEUE_NUM_5	See bits[3:0]. This is for priority queue 4.
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_5	See bits[3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_5	See bits[3:0]. This is for priority queue 2.

Table 5-223 PORT5_HOL_CTRL0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_5	See bits[3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_5	Most buffer can be used for priority 0 queue. Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.71 PORT5_HOL_CTRL1

Address offset: 0x099c

Table 5-224 summarizes the port 5 HOL control 1 register.

Table 5-224 PORT5_HOL_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:17	RO	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_5	Egress port mirror. If this bit is set to 1, all packets send out through this port are copied to mirror port.
15:9	RO	0	RESERVED	
8	R/W	1	PORT_RED_EN_1	WRED enable
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_5	1 = Enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_5	1 = Enable use PRI*_QUEUE_NUM to control queue depth in this port.
5:4	RO	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_5	Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.72 PORT6_HOL_CTRL0

Address offset: 0x09A0

Table 5-225 summarizes the port 6 HOL control 0 register.

Table 5-225 PORT6_HOL_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:30	RO	0	RESERVED	
29:24	R/W	0x2A	EG_PORT_QUEUE_NUM_6	Most buffer can be used for this port. Buffer number is times of 8. 6'h0: 0 6'h1: No more than 8 6'h2: No more than 16 6'h3F: No more than 504
23:20	R/W	0x8	EG_PRI5_QUEUE_NUM_6	See bits[3:0]. This is for priority queue 5.
19:16	R/W	0x8	EG_PRI4_QUEUE_NUM_6	See bits[3:0]. This is for priority queue 4.
15:12	R/W	0x8	EG_PRI3_QUEUE_NUM_6	See bits[3:0]. This is for priority queue 3.
11:8	R/W	0x8	EG_PRI2_QUEUE_NUM_6	See bits[3:0]. This is for priority queue 2.
7:4	R/W	0x8	EG_PRI1_QUEUE_NUM_6	See bits[3:0]. This is for priority queue 1.
3:0	R/W	0x8	EG_PRI0_QUEUE_NUM_6	Most buffer can be used for priority 0 queue. Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.73 PORT6_HOL_CTRL1

Address offset: 0x09A4

Table 5-226 summarizes the port 6 HOL control 1 register.

Table 5-226 PORT6_HOL_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:17	RO	0	RESERVED	
16	R/W	0	EG_MIRROR_EN_6	Egress port mirror. If this bit is set to 1, all packets send out through this port are copied to mirror port.
15:9	RO	0	RESERVED	
8	R/W	1	PORT_RED_EN_1	WRED enable
7	R/W	0x1	EG_PORT_QUEUE_CTRL_EN_6	1 = Enable use PORT_QUEUE_NUM to control queue depth in this port.
6	R/W	0x1	EG_PRI_QUEUE_CTRL_EN_6	1 = Enable use PRI*_QUEUE_NUM to control queue depth in this port.

Table 5-226 PORT6_HOL_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
5:4	RO	0	RESERVED	
3:0	R/W	4'h6	ING_BUF_NUM_6	Buffer number is times of 8. 4'h0: 0 4'h1: No more than 8 4'h2: No more than 16 4'hF: No more than 240

5.7.74 PORT0_FLOW_THD

Address offset: 0x09B0

Table 5-227 summarizes the port 0 flow control threshold control register.

Table 5-227 PORT0_FLOW_THD bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_0	Port-based transmit on threshold. When block memory used by one port is less than this value, MAC sends out pause off frame, and link partner starts transmitting frame out.
15:8	RO	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_0	Port-based transmit off threshold. When block memory used by one port is more than this value, MAC sends out pause on frame, and link partner stops transmitting frame out.

5.7.75 PORT1_FLOW_THD

Address offset: 0x09B4

Table 5-228 summarizes the port 1 flow control threshold control register.

Table 5-228 PORT1_FLOW_THD bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_1	Port-based transmit on threshold. When block memory used by one port is less than this value, MAC sends out pause off frame, and link partner starts transmitting frame out.

Table 5-228 PORT1_FLOW_THD bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
15:8	RO	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_1	Port-based transmit off threshold. When block memory used by one port is more than this value, MAC sends out pause on frame, and link partner stops transmitting frame out.

5.7.76 PORT2_FLOW_THD

Address offset: 0x09B8

[Table 5-229](#) summarizes the port 2 flow control threshold register.

Table 5-229 PORT2_FLOW_THD bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_2	Port-based transmit on threshold. When block memory used by one port is less than this value, MAC sends out pause off frame, and link partner starts transmitting frame out.
15:8	RO	0	RESERVED	
7:0	R/W	'h4B	PORT_XOFF_THRES_2	Port-based transmit off threshold. When block memory used by one port is more than this value, MAC sends out pause on frame, and link partner stops transmitting frame out.

5.7.77 PORT3_FLOW_THD

Address offset: 0x09BC

[Table 5-230](#) summarizes the port 3 flow control threshold control register.

Table 5-230 PORT3_FLOW_THD bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_3	Port-based transmit on threshold. When block memory used by one port is less than this value, MAC sends out pause off frame, and link partner starts transmitting frame out.

Table 5-230 PORT3_FLOW_THD bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
15:8	RO	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_3	Port-based transmit off threshold. When block memory used by one port is more than this value, MAC sends out pause on frame, and link partner stops transmitting frame out.

5.7.78 PORT4_FLOW_THD

Address offset: 0x09C0

Table 5-231 summarizes the port 4 flow control threshold control register.

Table 5-231 PORT4_FLOW_THD bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_4	Port-based transmit on threshold. When block memory used by one port is less than this value, MAC sends out pause off frame, and link partner starts transmitting frame out.
15:8	RO	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_4	Port-based transmit off threshold. When block memory used by one port is more than this value, MAC sends out pause on frame, and link partner stops transmitting frame out.

5.7.79 PORT5_FLOW_THD

Address offset: 0x09C4

Table 5-232 summarizes the port 5 flow control threshold control register.

Table 5-232 PORT5_FLOW_THD bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_5	Port-based transmit on threshold. When block memory used by one port is less than this value, MAC sends out pause off frame, and link partner starts transmitting frame out.

Table 5-232 PORT5_FLOW_THD bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
15:8	RO	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_5	Port-based transmit off threshold. When block memory used by one port is more than this value, MAC sends out pause on frame, and link partner stops transmitting frame out.

5.7.80 PORT6_FLOW_THD

Address offset: 0x09C8

Table 5-233 summarizes the port 6 flow control threshold control register.

Table 5-233 PORT6_FLOW_THD bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23:16	R/W	'h3A	PORT_XON_THRES_6	Port-based transmit on threshold. When block memory used by one port is less than this value, MAC sends out pause off frame, and link partner starts transmitting frame out.
15:8	RO	0	RESERVED	
7:0	R/W	'h4A	PORT_XOFF_THRES_6	Port-based transmit off threshold. When block memory used by one port is more than this value, MAC sends out pause on frame, and link partner stops transmitting frame out.

5.7.81 ACL_POLICY_MODE

Address offset: 0x09F0

Table 5-234 summarizes the ACL policy register.

Table 5-234 ACL_POLICY_MODE bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	ACL_SEL_31	See bit[0]
30	R/W	0	ACL_SEL_30	See bit[0]
29	R/W	0	ACL_SEL_29	See bit[0]
28	R/W	0	ACL_SEL_28	See bit[0]
27	R/W	0	ACL_SEL_27	See bit[0]
26	R/W	0	ACL_SEL_26	See bit[0]

Table 5-234 ACL_POLICY_MODE bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
25	R/W	0	ACL_SEL_25	See bit[0]
24	R/W	0	ACL_SEL_24	See bit[0]
23	R/W	0	ACL_SEL_23	See bit[0]
22	R/W	0	ACL_SEL_22	See bit[0]
21	R/W	0	ACL_SEL_21	See bit[0]
20	R/W	0	ACL_SEL_20	See bit[0]
19	R/W	0	ACL_SEL_19	See bit[0]
18	R/W	0	ACL_SEL_18	See bit[0]
17	R/W	0	ACL_SEL_17	See bit[0]
16	R/W	0	ACL_SEL_16	See bit[0]
15	R/W	0	ACL_SEL_15	See bit[0]
14	R/W	0	ACL_SEL_14	See bit[0]
13	R/W	0	ACL_SEL_13	See bit[0]
12	R/W	0	ACL_SEL_12	See bit[0]
11	R/W	0	ACL_SEL_11	See bit[0]
10	R/W	0	ACL_SEL_10	See bit[0]
9	R/W	0	ACL_SEL_9	See bit[0]
8	R/W	0	ACL_SEL_8	See bit[0]
7	R/W	0	ACL_SEL_7	See bit[0]
6	R/W	0	ACL_SEL_6	See bit[0]
5	R/W	0	ACL_SEL_5	See bit[0]
4	R/W	0	ACL_SEL_4	See bit[0]
3	R/W	0	ACL_SEL_3	See bit[0]
2	R/W	0	ACL_SEL_2	See bit[0]
1	R/W	0	ACL_SEL_1	See bit[0]
0	R/W	0	ACL_SEL_0	0 = ACL rate limit 1 = ACL counter

5.7.82 ACL_COUNTER_MODE

Address offset: 0x09F4

Table 5-235 summarizes the ACL counter mode register.

Table 5-235 ACL_COUNTER_MODE bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	ACL_CNT_MODE_31	See bit[0]
30	R/W	0	ACL_CNT_MODE_30	See bit[0]
29	R/W	0	ACL_CNT_MODE_29	See bit[0]
28	R/W	0	ACL_CNT_MODE_28	See bit[0]
27	R/W	0	ACL_CNT_MODE_27	See bit[0]
26	R/W	0	ACL_CNT_MODE_26	See bit[0]
25	R/W	0	ACL_CNT_MODE_25	See bit[0]
24	R/W	0	ACL_CNT_MODE_24	See bit[0]
23	R/W	0	ACL_CNT_MODE_23	See bit[0]
22	R/W	0	ACL_CNT_MODE_22	See bit[0]
21	R/W	0	ACL_CNT_MODE_21	See bit[0]
20	R/W	0	ACL_CNT_MODE_20	See bit[0]
19	R/W	0	ACL_CNT_MODE_19	See bit[0]
18	R/W	0	ACL_CNT_MODE_18	See bit[0]
17	R/W	0	ACL_CNT_MODE_17	See bit[0]
16	R/W	0	ACL_CNT_MODE_16	See bit[0]
15	R/W	0	ACL_CNT_MODE_15	See bit[0]
14	R/W	0	ACL_CNT_MODE_14	See bit[0]
13	R/W	0	ACL_CNT_MODE_13	See bit[0]
12	R/W	0	ACL_CNT_MODE_12	See bit[0]
11	R/W	0	ACL_CNT_MODE_11	See bit[0]
10	R/W	0	ACL_CNT_MODE_10	See bit[0]
9	R/W	0	ACL_CNT_MODE_9	See bit[0]
8	R/W	0	ACL_CNT_MODE_8	See bit[0]
7	R/W	0	ACL_CNT_MODE_7	See bit[0]
6	R/W	0	ACL_CNT_MODE_6	See bit[0]
5	R/W	0	ACL_CNT_MODE_5	See bit[0]
4	R/W	0	ACL_CNT_MODE_4	See bit[0]
3	R/W	0	ACL_CNT_MODE_3	See bit[0]
2	R/W	0	ACL_CNT_MODE_2	See bit[0]
1	R/W	0	ACL_CNT_MODE_1	See bit[0]
0	R/W	0	ACL_CNT_MODE_0	0 = Frame counter 1 = Byte counter

5.7.83 ACL_CNT_RESET

Address offset: 0x09F8

Table 5-236 summarizes the ACL counter reset register.

Table 5-236 ACL_CNT_RESET bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	ACL_CNT_RST_31	See bit[0]
30	R/W	0	ACL_CNT_RST_30	See bit[0]
29	R/W	0	ACL_CNT_RST_29	See bit[0]
28	R/W	0	ACL_CNT_RST_28	See bit[0]
27	R/W	0	ACL_CNT_RST_27	See bit[0]
26	R/W	0	ACL_CNT_RST_26	See bit[0]
25	R/W	0	ACL_CNT_RST_25	See bit[0]
24	R/W	0	ACL_CNT_RST_24	See bit[0]
23	R/W	0	ACL_CNT_RST_23	See bit[0]
22	R/W	0	ACL_CNT_RST_22	See bit[0]
21	R/W	0	ACL_CNT_RST_21	See bit[0]
20	R/W	0	ACL_CNT_RST_20	See bit[0]
19	R/W	0	ACL_CNT_RST_19	See bit[0]
18	R/W	0	ACL_CNT_RST_18	See bit[0]
17	R/W	0	ACL_CNT_RST_17	See bit[0]
16	R/W	0	ACL_CNT_RST_16	See bit[0]
15	R/W	0	ACL_CNT_RST_15	See bit[0]
14	R/W	0	ACL_CNT_RST_14	See bit[0]
13	R/W	0	ACL_CNT_RST_13	See bit[0]
12	R/W	0	ACL_CNT_RST_12	See bit[0]
11	R/W	0	ACL_CNT_RST_11	See bit[0]
10	R/W	0	ACL_CNT_RST_10	See bit[0]
9	R/W	0	ACL_CNT_RST_9	See bit[0]
8	R/W	0	ACL_CNT_RST_8	See bit[0]
7	R/W	0	ACL_CNT_RST_7	See bit[0]
6	R/W	0	ACL_CNT_RST_6	See bit[0]
5	R/W	0	ACL_CNT_RST_5	See bit[0]
4	R/W	0	ACL_CNT_RST_4	See bit[0]
3	R/W	0	ACL_CNT_RST_3	See bit[0]
2	R/W	0	ACL_CNT_RST_2	See bit[0]

Table 5-236 ACL_CNT_RESET bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
1	R/W	0	ACL_CNT_RST_1	See bit[0]
0	R/W	0	ACL_CNT_RST_0	1 = Clear counter

5.7.84 ACL_RATE_CTRL0_0

Address offset: 0x0A00

Table 5-237 summarizes the ACL 0 rate control 0 register.

Table 5-237 ACL_RATE_CTRL0_0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_0	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_0	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.85 ACL_RATE_CTRL1_0

Address offset: 0x0A04

Table 5-238 summarizes the ACL0 rate control 1 register.

Table 5-238 ACL_RATE_CTRL1_0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_0	Borrow enable
22	R/W	0	ACL_RATE_UNIT_0	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_0	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_0	Color mode for ingress rate limit

Table 5-238 ACL_RATE_CTRL1_0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
19:18	R/W	01	ACL_RATE_TIME_SLOT_0	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_0	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_0	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.86 ACL_RATE_CTRL0_1

Address offset: 0x0A08

Table 5-239 summarizes the ACL 1 rate control 0 register.

Table 5-239 ACL_RATE_CTRL0_1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_1	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_1	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.87 ACL_RATE_CTRL1_1

Address offset: 0x0A0C

Table 5-240 summarizes the ACL 1 rate control 1 register.

Table 5-240 ACL_RATE_CTRL1_1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_1	Borrow enable
22	R/W	0	ACL_RATE_UNIT_1	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_1	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_1	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_1	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_1	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_1	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.88 ACL_RATE_CTRL0_2

Address offset: 0x0A10

Table 5-241 summarizes the ACL 2 rate control 0 register.

Table 5-241 ACL_RATE_CTRL0_2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_2	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_2	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.89 ACL_RATE_CTRL1_2

Address offset: 0x0A14

Table 5-242 summarizes the ACL 2 rate control 1 register.

Table 5-242 ACL_RATE_CTRL1_2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_2	Borrow enable
22	R/W	0	ACL_RATE_UNIT_2	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_2	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_2	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_2	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_2	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_2	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.90 ACL_RATE_CTRL0_3

Address offset: 0x0A18

Table 5-243 summarizes the ACL 3 rate control 0 register.

Table 5-243 ACL_RATE_CTRL0_3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_3	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_3	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.91 ACL_RATE_CTRL1_3

Address offset: 0x0A1C

Table 5-244 summarizes the ACL 3 rate control 1 register.

Table 5-244 ACL_RATE_CTRL1_3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_3	Borrow enable
22	R/W	0	ACL_RATE_UNIT_3	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_3	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_3	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_3	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_3	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_3	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.92 ACL_RATE_CTRL0_4

Address offset: 0x0A20

Table 5-245 summarizes the ACL 4 rate control 0 register.

Table 5-245 ACL_RATE_CTRL0_4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_4	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_4	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.93 ACL_RATE_CTRL1_4

Address offset: 0x0A24

Table 5-246 summarizes the ACL 4 rate control 1 register.

Table 5-246 ACL_RATE_CTRL1_4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_4	Borrow enable
22	R/W	0	ACL_RATE_UNIT_4	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_4	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_4	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_4	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ACL_EBS_4	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_4	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.94 ACL_RATE_CTRL0_5

Address offset: 0x0A28

Table 5-247 summarizes the ACL 5 rate control 0 register.

Table 5-247 ACL_RATE_CTRL0_5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_5	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_5	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.95 ACL_RATE_CTRL1_5

Address offset: 0x0A2C

Table 5-248 summarizes the ACL 5 rate control 1 register.

Table 5-248 ACL_RATE_CTRL1_5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_5	Borrow enable
22	R/W	0	ACL_RATE_UNIT_5	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_5	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_5	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_5	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ACL_EBS_5	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_5	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.96 ACL_RATE_CTRL0_6

Address offset: 0x0A30

Table 5-249 summarizes the ACL 6 rate control 0 register.

Table 5-249 ACL_RATE_CTRL0_6 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_6	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_6	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.97 ACL_RATE_CTRL1_6

Address offset: 0x0A34

Table 5-250 summarizes the ACL 6 rate control 1 register.

Table 5-250 ACL_RATE_CTRL1_6 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_6	Borrow enable
22	R/W	0	ACL_RATE_UNIT_6	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_6	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_6	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_6	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96kbps, do not select 100us as time slot
17:15	R/W	0	ACL_EBS_6	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_6	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.98 ACL_RATE_CTRL0_7

Address offset: 0x0A38

Table 5-251 summarizes the ACL 7 rate limit control 0 register.

Table 5-251 ACL_RATE_CTRL0_7 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_7	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_7	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.99 ACL_RATE_CTRL1_7

Address offset: 0x0A3C

Table 5-252 summarizes the ACL 7 rate control 1 register.

Table 5-252 ACL_RATE_CTRL1_7 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_7	Borrow enable
22	R/W	0	ACL_RATE_UNIT_7	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_7	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_7	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_7	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_7	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_7	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.100 ACL_RATE_CTRL0_8

Address offset: 0x0A40

Table 5-253 summarizes the ACL 8 rate control 0 register.

Table 5-253 ACL_RATE_CTRL0_8 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_8	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_8	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.101 ACL_RATE_CTRL1_8

Address offset: 0x0A44

Table 5-254 summarizes the ACL8 rate control 1 register.

Table 5-254 ACL_RATE_CTRL1_8 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_8	Borrow enable
22	R/W	0	ACL_RATE_UNIT_8	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_8	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_8	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_8	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_8	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_8	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.102 ACL_RATE_CTRL0_9

Address offset: 0x0A48

Table 5-255 summarizes the ACL9 rate control 0 register.

Table 5-255 ACL_RATE_CTRL0_9 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_9	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_9	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.103 ACL_RATE_CTRL1_9

Address offset: 0x0A4C

Table 5-256 summarizes the ACL 9 rate control 1 register.

Table 5-256 ACL_RATE_CTRL1_9 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_9	Borrow enable
22	R/W	0	ACL_RATE_UNIT_9	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_9	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_9	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_9	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_9	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_9	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.104 ACL_RATE_CTRL0_10

Address 0x0A50

Table 5-257 summarizes the ACL 10 rate control 0 register.

Table 5-257 ACL_RATE_CTRL0_10 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_10	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_10	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.105 ACL_RATE_CTRL1_10

Address offset: 0x0A54

Table 5-258 summarizes the ACL 10 rate control 1 register.

Table 5-258 ACL_RATE_CTRL1_10 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_10	Borrow enable
22	R/W	0	ACL_RATE_UNIT_10	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_10	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_10	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_10	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_10	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_10	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.106 ACL_RATE_CTRL0_11

Address offset: 0x0A58

Table 5-259 summarizes the ACL 11 rate control 0 register.

Table 5-259 ACL_RATE_CTRL0_11 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_11	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_11	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.107 ACL_RATE_CTRL1_11

Address offset: 0x0A5C

Table 5-260 summarizes the ACL 11 rate control 1 register.

Table 5-260 ACL_RATE_CTRL1_11 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_11	Borrow enable
22	R/W	0	ACL_RATE_UNIT_11	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_11	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_11	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_11	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_11	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_11	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.108 ACL_RATE_CTRL0_12

Address offset: 0x0A60

Table 5-261 summarizes the ACL 12 rate control 0 register.

Table 5-261 ACL_RATE_CTRL0_12 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_12	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_12	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.109 ACL_RATE_CTRL1_12

Address offset: 0x0A64

Table 5-262 summarizes the ACL 12 rate control 1 register.

Table 5-262 ACL_RATE_CTRL1_12 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_12	Borrow enable
22	R/W	0	ACL_RATE_UNIT_12	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_12	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_12	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_12	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ACL_EBS_12	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_12	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.110 ACL_RATE_CTRL0_13

Address offset: 0x0A68

Table 5-263 summarizes the ACL 13 rate control 0 register.

Table 5-263 ACL_RATE_CTRL0_13 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_13	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_13	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.111 ACL_RATE_CTRL1_13

Address offset: 0x0A6C

Table 5-264 summarizes the ACL 13 rate control 1 register.

Table 5-264 ACL_RATE_CTRL1_13 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_13	Borrow enable
22	R/W	0	ACL_RATE_UNIT_13	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_13	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_13	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_13	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_13	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_13	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.112 ACL_RATE_CTRL0_14

Address offset: 0x0A70

Table 5-265 summarizes the ACL 14 rate control 0 register.

Table 5-265 ACL_RATE_CTRL0_14 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_14	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_14	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.113 ACL_RATE_CTRL1_14

Address offset: 0x0A74

Table 5-266 summarizes the ACL 14 rate control 1 register.

Table 5-266 ACL_RATE_CTRL1_14 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_14	Borrow enable
22	R/W	0	ACL_RATE_UNIT_14	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_14	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_14	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_14	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ACL_EBS_14	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_14	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.114 ACL_RATE_CTRL0_15

Address offset: 0x0A78

Table 5-267 summarizes the ACL 15 rate limit control 0 register.

Table 5-267 ACL_RATE_CTRL0_15 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_15	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_15	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.115 ACL_RATE_CTRL1_15

Address offset: 0x0A7C

Table 5-268 summarizes the ACL 15 rate limit control 1 register.

Table 5-268 ACL_RATE_CTRL1_15 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_15	Borrow enable
22	R/W	0	ACL_RATE_UNIT_15	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_15	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_15	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_15	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_15	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_15	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.116 ACL_RATE_CTRL0_16

Address offset: 0x0A80

Table 5-269 summarizes the ACL 16 rate limit control 0 register.

Table 5-269 ACL_RATE_CTRL0_16 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_16	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_16	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.117 ACL_RATE_CTRL1_16

Address offset: 0x0A84

Table 5-270 summarizes the ACL 16 rate limit control 1 register.

Table 5-270 ACL_RATE_CTRL1_16 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_16	Borrow enable
22	R/W	0	ACL_RATE_UNIT_16	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_16	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_16	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_16	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_16	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_16	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.118 ACL_RATE_CTRL0_17

Address offset: 0x0A88

Table 5-271 summarizes the ACL 17 rate limit control 0 register.

Table 5-271 ACL_RATE_CTRL1_17 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_17	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_17	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.119 ACL_RATE_CTRL1_17

Address offset: 0x0A8C

Table 5-272 summarizes the ACL 17 rate limit control 1 register.

Table 5-272 ACL_RATE_CTRL1_17 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_17	Borrow enable
22	R/W	0	ACL_RATE_UNIT_17	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_17	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_17	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_17	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_17	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_17	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.120 ACL_RATE_CTRL0_18

Address offset: 0x0A90

Table 5-273 summarizes the ACL 18 rate limit control 0 register.

Table 5-273 ACL_RATE_CTRL0_18 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_18	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_18	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.121 ACL_RATE_CTRL0_18

Address offset: 0x0A94

Table 5-274 summarizes the ACL 18 rate limit control 0 register.

Table 5-274 ACL_RATE_CTRL1_18 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_18	Borrow enable
22	R/W	0	ACL_RATE_UNIT_18	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_18	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_18	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_18	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ACL_EBS_18	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_18	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.122 ACL_RATE_CTRL0_19

Address offset: 0x0A98

Table 5-275 summarizes the ACL 19 rate limit control 0 register.

Table 5-275 ACL_RATE_CTRL0_19 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_19	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_19	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.123 ACL_RATE_CTRL1_19

Address offset: 0x0A9C

Table 5-276 summarizes the ACL 19 rate limit control 1 register.

Table 5-276 ACL_RATE_CTRL1_19 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_19	Borrow enable
22	R/W	0	ACL_RATE_UNIT_19	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_19	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_19	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_19	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_19	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_19	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.124 ACL_RATE_CTRL0_20

Address offset: 0x0AA0

Table 5-277 summarizes the ACL 20 rate limit control 0 register.

Table 5-277 ACL_RATE_CTRL0_20 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_20	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_20	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.125 ACL_RATE_CTRL1_20

Address offset: 0x0AA4

Table 5-278 summarizes the ACL 20 rate limit control 1 register.

Table 5-278 ACL_RATE_CTRL1_20 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_20	Borrow enable
22	R/W	0	ACL_RATE_UNIT_20	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_20	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_20	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_20	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ACL_EBS_20	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_20	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.126 ACL_RATE_CTRL0_21

Address offset: 0x0AA8

Table 5-279 summarizes the ACL 21 rate limit control 0 register.

Table 5-279 ACL_RATE_CTRL0_21 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_21	Committed burst size for ingress rate limit
14:0	R/W	0	ACL_CIR_21	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.127 ACL_RATE_CTRL1_21

Address offset: 0x0AAC

Table 5-280 summarizes the ACL 21 rate limit control 1 register.

Table 5-280 ACL_RATE_CTRL1_21 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_21	Borrow enable
22	R/W	0	ACL_RATE_UNIT_21	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_21	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_21	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_21	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_21	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_21	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.128 ACL_RATE_CTRL0_22

Address offset: 0x0AB0

Table 5-281 summarizes the ACL 22 rate limit control 0 register.

Table 5-281 ACL_RATE_CTRL0_22 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	

Table 5-281 ACL_RATE_CTRL0_22 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
17:15	R/W	0	ACL_CBS_22	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_22	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.129 ACL_RATE_CTRL1_22

Address offset: 0x0AB4

Table 5-282 summarizes the ACL 22 rate limit control 1 register.

Table 5-282 ACL_RATE_CTRL1_22 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_22	Borrow enable
22	R/W	0	ACL_RATE_UNIT_22	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_22	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_22	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_22	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_22	Excess burst size for ingress rate limit
14:0	R/W	0X7FFF	ACL_EIR_22	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.130 ACL_RATE_CTRL0_23

Address offset: 0x0AB8

Table 5-283 summarizes the ACL 23 rate limit control 0 register.

Table 5-283 ACL_RATE_CTRL0_23 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_23	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_23	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.131 ACL_RATE_CTRL1_23

Address offset: 0x0ABC

Table 5-284 summarizes the ACL 23 rate limit control 1 register.

Table 5-284 ACL_RATE_CTRL1_23 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_23	Borrow enable
22	R/W	0	ACL_RATE_UNIT_23	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_23	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_23	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_23	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_23	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_23	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.132 ACL_RATE_CTRL0_24

Address offset: 0x0AC0

Table 5-285 summarizes the ACL 24 rate limit control 0 register.

Table 5-285 ACL_RATE_CTRL0_24 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_24	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_24	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.133 ACL_RATE_CTRL1_24

Address offset: 0x0AC4

Table 5-286 summarizes the ACL 24 rate limit control 1 register.

Table 5-286 ACL_RATE_CTRL1_24 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_24	Borrow enable
22	R/W	0	ACL_RATE_UNIT_24	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_24	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_24	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_24	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_24	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_24	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.134 ACL_RATE_CTRL0_25

Address offset: 0x0AC8

Table 5-287 summarizes the ACL 25 rate limit control register 0.

Table 5-287 ACL_RATE_CTRL0_25 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_25	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_25	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.135 ACL_RATE_CTRL1_25

Address offset: 0x0ACC

Table 5-288 summarizes the ACL 25 rate limit control 1 register.

Table 5-288 ACL_RATE_CTRL1_25 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_25	Borrow enable
22	R/W	0	ACL_RATE_UNIT_25	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_25	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_25	Color mode for ingress rate limit
19:18	RO	01	ACL_RATE_TIME_SLOT_25	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_25	Excess burst size for ingress rate limit
14:0	RO	0x7FFF	ACL_EIR_25	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.136 ACL_RATE_CTRL0_26

Address offset: 0x0AD0

Table 5-289 summarizes the ACL 26 rate limit control 0 register.

Table 5-289 ACL_RATE_CTRL0_26 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_26	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_26	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.137 ACL_RATE_CTRL1_26

Address offset: 0x0AD4

Table 5-290 summarizes the ACL 26 rate limit control 1 register.

Table 5-290 ACL_RATE_CTRL1_26 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_26	Borrow enable
22	R/W	0	ACL_RATE_UNIT_26	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_26	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_26	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_26	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_26	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_26	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.138 ACL_RATE_CTRL0_27

Address offset: 0x0AD8

Table 5-291 summarizes the ACL 27 rate limit control 0 register.

Table 5-291 ACL_RATE_CTRL0_27 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_27	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_27	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.139 ACL_RATE_CTRL1_27

Address offset: 0x0ADC

Table 5-292 summarizes the ACL 27 rate limit control 1 register.

Table 5-292 ACL_RATE_CTRL1_27 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_27	Borrow enable
22	R/W	0	ACL_RATE_UNIT_27	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_27	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_27	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_27	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_27	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_27	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.140 ACL_RATE_CTRL0_28

Address offset: 0x0AE0

Table 5-293 summarizes the ACL 28 rate limit control 0 register.

Table 5-293 ACL_RATE_CTRL0_28 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_28	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_28	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.141 ACL_RATE_CTRL1_28

Address offset: 0x0AE4

Table 5-294 summarizes the ACL 28 rate limit control 1 register.

Table 5-294 ACL_RATE_CTRL1_28 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_28	Borrow enable
22	R/W	0	ACL_RATE_UNIT_28	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_28	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_28	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_28	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_28	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_28	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.142 ACL_RATE_CTRL0_29

Address offset: 0x0AE8

Table 5-295 summarizes the ACL 29 rate limit control 0 register.

Table 5-295 ACL_RATE_CTRL0_29 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_29	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_29	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.143 ACL_RATE_CTRL1_29

Address offset: 0x0AEC

Table 5-296 summarizes the ACL 29 rate limit control 1 register.

Table 5-296 ACL_RATE_CTRL1_29 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_29	Borrow enable
22	R/W	0	ACL_RATE_UNIT_29	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_29	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_29	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_29	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_29	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_29	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.144 ACL_RATE_CTRL0_30

Address offset: 0x0AF0

Table 5-297 summarizes the ACL 30 rate limit control 0 register.

Table 5-297 ACL_RATE_CTRL0_30 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_30	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_30	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.145 ACL_RATE_CTRL1_30

Address offset: 0x0AF4

Table 5-298 summarizes the ACL 30 rate limit control 1 register.

Table 5-298 ACL_RATE_CTRL1_30 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_30	Borrow enable
22	R/W	0	ACL_RATE_UNIT_30	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_30	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_30	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_30	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot
17:15	R/W	0	ACL_EBS_30	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_30	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.146 ACL_RATE_CTRL0_31

Address offset: 0x0AF8

Table 5-299 summarizes the ACL 31 rate limit control 0 register.

Table 5-299 ACL_RATE_CTRL0_31 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:18	RO	0	RESERVED	
17:15	R/W	0	ACL_CBS_31	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_CIR_31	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.147 ACL_RATE_CTRL1_31

Address offset: 0x0AFC

Table 5-300 summarizes the ACL 31 rate limit control 1 register.

Table 5-300 ACL_RATE_CTRL1_31 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ACL_BORROW_EN_31	Borrow enable
22	R/W	0	ACL_RATE_UNIT_31	0 = Bytes 1 = Packets
21	R/W	0	ACL_CF_31	Coupling flag for ingress rate limit
20	R/W	0	ACL_CM_31	Color mode for ingress rate limit
19:18	R/W	01	ACL_RATE_TIME_SLOT_31	ACL ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ACL_EBS_31	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ACL_EIR_31	Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.148 PORT0_ING_RATE_CTRL0

Address offset: 0x0B00

Table 5-301 summarizes the port 0 ingress rate limit control 0 register.

Table 5-301 PORT0_ING_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_0	Byte number is added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, CRC and SFD.
23:22	R/W	01	ING_RATE_C_TIME_SLOT_0	Committed Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
21	RO	0	RESERVED	
20	R/W	0	ING_RATE_MODE_0	0 = Two single rate 1 = One two-rate three-color
19:18	RO	0	RESERVED	
17:15	/W	0	ING_CBS_0	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_0	Committed Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.149 PORT0_ING_RATE_CTRL1

Address offset: 0x0B04

Table 5-302 summarizes the port 0 ingress rate limit control 1 register.

Table 5-302 PORT0_ING_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ING_BORROW_EN_0	Borrow enable
22	R/W	0	ING_RATE_UNIT_0	0 = Bytes 1 = Packets
21	R/W	0	ING_CF_0	Coupling flag for ingress rate limit

Table 5-302 PORT0_ING_RATE_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
20	R/W	0	ING_CM_0	Color mode for ingress rate limit
19:18	R/W	01	ING_RATE_E_TIME_SLOT_0	Excess Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ING_EBS_0	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_0	Excess Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.150 PORT0_ING_RATE_CTRL2

Address offset: 0x0B08

Table 5-303 summarizes the port 0 ingress rate limit control 2 register.

Table 5-303 PORT0_ING_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_0	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_0	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_0	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	0	ING_C_UNK_UNI_RATE_EN_0	Ingress committed rate limit enable to count the unknown unicast frames
11	R/W	0	ING_C_BROAD_RATE_EN_0	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_0	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_0	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_0	Ingress committed rate limit enable to count the ingress mirror frames

Table 5-303 PORT0_ING_RATE_CTRL2 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
7	R/W	0	ING_E_MULTI_RATE_EN_0	Ingress excess rate limit enable to count the multicast frames
6	R/W	0	ING_E_UNI_RATE_EN_0	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_0	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_0	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_0	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_0	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_0	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_0	Ingress excess rate limit enable to count the ingress mirror frames

5.7.151 PORT1_ING_RATE_CTRL0

Address offset: 0x0B10

Table 5-304 summarizes the port 1 ingress rate limit 0 control register.

Table 5-304 PORT1_ING_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_1	Byte number is added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, CRC and SFD.
23:22	R/W	01	ING_RATE_C_TIME_SLOT_1	Committed Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
21	RO	0	RESERVED	
20	R/W	0	ING_RATE_MODE_1	0 = Two single rate 1 = One two-rate three-color
19:18	RO	0	RESERVED	

Table 5-304 PORT1_ING_RATE_CTRL0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
17:15	R/W	0	ING_CBS_1	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_1	Committed Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no frame is received in from this port.

5.7.152 PORT1_ING_RATE_CTRL1

Address offset: 0x0B14

Table 5-305 summarizes the port 1 ingress rate limit control 1 register.

Table 5-305 PORT1_ING_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ING_BORROW_EN_1	Borrow enable
22	R/W	0	ING_RATE_UNIT_1	0 = Bytes 1 = Packets
21	R/W	0	ING_CF_1	Coupling flag for ingress rate limit
20	R/W	0	ING_CM_1	Color mode for ingress rate limit
19:18	R/W	01	ING_RATE_E_TIME_SLOT_1	Excess Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ING_EBS_1	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_1	Excess Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.153 PORT1_ING_RATE_CTRL2

Address offset: 0x0B18

Table 5-306 summarizes the port 1 ingress rate limit control 2 register.

Table 5-306 PORT1_ING_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_1	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_1	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_1	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	0	ING_C_UNK_UNI_RATE_EN_1	Ingress committed rate limit enable to count the unknown unicast frames
11	R/W	0	ING_C_BROAD_RATE_EN_1	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_1	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_1	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_1	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	0	ING_E_MULTI_RATE_EN_1	Ingress excess rate limit enable to count the multicast frames
6	R/W	0	ING_E_UNI_RATE_EN_1	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_1	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_1	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_1	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_1	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_1	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_1	Ingress excess rate limit enable to count the ingress mirror frames

5.7.154 PORT2_ING_RATE_CTRL0

Address offset: 0x0B20

[Table 5-307](#) summarizes the port 2 ingress rate limit control 0 register.

Table 5-307 PORT2_ING_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_2	Byte number is added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, CRC and SFD.
23:22	R/W	01	ING_RATE_C_TIME_SLOT_2	Committed Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
21	RO	0	RESERVED	
20	R/W	0	ING_RATE_MODE_2	0 = Two single rate 1 = One two-rate three-color
19:18	RO	0	RESERVED	
17:15	R/W	0	ING_CBS_2	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_2	Committed Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no frame is received in from this port.

5.7.155 PORT2_ING_RATE_CTRL1

Address offset: 0x0B24

Table 5-308 summarizes the port 2 ingress rate limit control 1 register.

Table 5-308 PORT2_ING_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ING_BORROW_EN_2	Borrow enable
22	R/W	0	ING_RATE_UNIT_2	0 = Bytes 1 = Packets
21	R/W	0	ING_CF_2	Coupling flag for ingress rate limit
20	R/W	0	ING_CM_2	Color mode for ingress rate limit

Table 5-308 PORT2_ING_RATE_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
19:18	R/W	01	ING_RATE_E_TIME_SLOT_2	Excess Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ING_EBS_2	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_2	Excess Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.156 PORT2_ING_RATE_CTRL2

Address offset: 0x0B28

Table 5-309 summarizes the port 2 ingress rate limit control 2 register.

Table 5-309 PORT2_ING_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_2	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_2	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_2	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	0	ING_C_UNK_UNI_RATE_EN_2	Ingress committed rate limit enable to count the unknown unicast frames
11	R/W	0	ING_C_BROAD_RATE_EN_2	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_2	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_2	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_2	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	0	ING_E_MULTI_RATE_EN_2	Ingress excess rate limit enable to count the multicast frames

Table 5-309 PORT2_ING_RATE_CTRL2 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
6	R/W	0	ING_E_UNI_RATE_EN_2	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_2	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_2	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_2	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_2	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_2	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_2	Ingress excess rate limit enable to count the ingress mirror frames

5.7.157 PORT3_ING_RATE_CTRL0

Address offset: 0x0B30

Table 5-310 summarizes the port 3 ingress rate limit control 0 register.

Table 5-310 PORT3_ING_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_3	Byte number is added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, CRC and SFD.
23:22	R/W	01	ING_RATE_C_TIME_SLOT_3	Committed Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
21	RO	0	RESERVED	
20	R/W	0	ING_RATE_MODE_3	0 = Two single rate 1 = One two-rate three-color
19:18	RO	0	RESERVED	

Table 5-310 PORT3_ING_RATE_CTRL0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
17:15	R/W	0	ING_CBS_3	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_3	Committed Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no frame is received in from this port.

5.7.158 PORT3_ING_RATE_CTRL1

Address offset: 0x0B34

Table 5-311 summarizes the port 3 ingress rate limit control 1 register.

Table 5-311 PORT3_ING_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ING_BORROW_EN_3	Borrow enable
22	R/W	0	ING_RATE_UNIT_3	0 = Bytes 1 = Packets
21	R/W	0	ING_CF_3	Coupling flag for ingress rate limit
20	R/W	0	ING_CM_3	Color mode for ingress rate limit
19:18	R/W	01	ING_RATE_E_TIME_SLOT_3	Excess Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ING_EBS_3	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_3	Excess Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.159 PORT3_ING_RATE_CTRL2

Address offset: 0x0B38

Table 5-312 summarizes the port 3 ingress rate limit control 2 register.

Table 5-312 PORT3_ING_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_3	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_3	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_3	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	0	ING_C_UNK_UNI_RATE_EN_3	Ingress committed rate limit enable to count the unknown unicast frames
11	R/W	0	ING_C_BROAD_RATE_EN_3	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_3	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_3	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_3	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	0	ING_E_MULTI_RATE_EN_3	Ingress excess rate limit enable to count the multicast frames
6	R/W	0	ING_E_UNI_RATE_EN_3	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_3	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_3	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_3	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_3	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_3	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_3	Ingress excess rate limit enable to count the ingress mirror frames

5.7.160 PORT4_ING_RATE_CTRL0

Address offset: 0x0B40

Table 5-313 summarizes the port 4 ingress rate limit control 0 register.

Table 5-313 PORT4_ING_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	'h18	ADD_RATE_BYTE_4	Byte number is added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, CRC and SFD.
23:22	R/W	01	ING_RATE_C_TIME_SLOT_4	Committed Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
21	R/W	0	RESERVED	
20	R/W	0	ING_RATE_MODE_4	0 = Two single rate 1 = One two-rate three-color
19:18	R/W	0	RESERVED	
17:15	R/W	0	ING_CBS_4	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_4	Committed Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no frame is received in from this port.

5.7.161 PORT4_ING_RATE_CTRL1

Address offset: 0x0B44

Table 5-314 summarizes the port 4 ingress rate limit control 1 register.

Table 5-314 PORT4_ING_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ING_BORROW_EN_4	Borrow enable
22	R/W	0	ING_RATE_UNIT_4	0 = Bytes 1 = Packets
21	R/W	0	ING_CF_4	Coupling flag for ingress rate limit
20	R/W	0	ING_CM_4	Color mode for ingress rate limit

Table 5-314 PORT4_ING_RATE_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
19:18	R/W	01	ING_RATE_E_TIME_SLOT_4	Excess Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ING_EBS_4	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_4	Excess Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.162 PORT4_ING_RATE_CTRL2

Address offset: 0x0B48

Table 5-315 summarizes the port 4 ingress rate limit control 2 register.

Table 5-315 PORT4_ING_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_4	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_4	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_4	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	0	ING_C_UNK_UNI_RATE_EN_4	Ingress committed rate limit enable to count the unknown unicast frames
11	R/W	0	ING_C_BROAD_RATE_EN_4	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_4	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_4	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_4	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	0	ING_E_MULTI_RATE_EN_4	Ingress excess rate limit enable to count the multicast frames

Table 5-315 PORT4_ING_RATE_CTRL2 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
6	R/W	0	ING_E_UNI_RATE_EN_4	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_4	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_4	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_4	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_4	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_4	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_4	Ingress excess rate limit enable to count the ingress mirror frames

5.7.163 PORT5_ING_RATE_CTRL0

Address offset: 0x0B50

Table 5-316 summarizes the port 5 ingress rate limit control 0 register.

Table 5-316 PORT5_ING_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_5	Byte number is added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, CRC and SFD.
23:22	R/W	01	ING_RATE_C_TIME_SLOT_5	Committed Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
21	RO	0	RESERVED	
20	R/W	0	ING_RATE_MODE_5	0 = Two single rate 1 = One two-rate three-color
19:18	RO	0	RESERVED	

Table 5-316 PORT5_ING_RATE_CTRL0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
17:15	R/W	0	ING_CBS_5	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_5	Committed Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no frame is received in from this port.

5.7.164 PORT5_ING_RATE_CTRL1

Address offset: 0x0B54

Table 5-317 summarizes the port 5 ingress rate limit control 1 register.

Table 5-317 PORT5_ING_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	0	RESERVED	
23	R/W	0	ING_BORROW_EN_5	Borrow enable
22	R/W	0	ING_RATE_UNIT_5	0 = Bytes 1 = Packets
21	R/W	0	ING_CF_5	Coupling flag for ingress rate limit
20	R/W	0	ING_CM_5	Color mode for ingress rate limit
19:18	R/W	01	ING_RATE_E_TIME_SLOT_5	Excess Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ING_EBS_5	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_5	Excess Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.165 PORT5_ING_RATE_CTRL2

Address offset: 0x0B58

Table 5-318 summarizes the port 5 ingress rate limit control 2 register.

Table 5-318 PORT5_ING_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_5	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_5	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_5	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	0	ING_C_UNK_UNI_RATE_EN_5	Ingress committed rate limit enable to count the unknown unicast frames
11	R/W	0	ING_C_BROAD_RATE_EN_5	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_5	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_5	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_5	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	0	ING_E_MULTI_RATE_EN_5	Ingress excess rate limit enable to count the multicast frames
6	R/W	0	ING_E_UNI_RATE_EN_5	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_5	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_5	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_5	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_5	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_5	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_5	Ingress excess rate limit enable to count the ingress mirror frames

5.7.166 PORT6_ING_RATE_CTRL0

Address offset: 0x0B60

Table 5-319 summarizes the port 6 ingress rate limit control 0 register.

Table 5-319 PORT6_ING_RATE_CTRL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	R/W	'h18	ADD_RATE_BYTE_6	Byte number is added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, CRC and SFD.
23:22	R/W	01	ING_RATE_C_TIME_SLOT_6	Committed Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
21	RO	0	RESERVED	
20	R/W	0	ING_RATE_MODE_6	0 = Two single rate 1 = One two-rate three-color
19:18	RO	0	RESERVED	
17:15	R/W	0	ING_CBS_6	Committed burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_CIR_6	Committed Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for egress priority 2. If these bits are set to 15'h0, no frame is received in from this port.

5.7.167 PORT6_ING_RATE_CTRL1

Address offset: 0x0B64

Table 5-320 summarizes the port 6 ingress rate limit control 1 register.

Table 5-320 PORT6_ING_RATE_CTRL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:24	RO	'h18	RESERVED	
23	R/W	0	ING_BORROW_EN_6	Borrow enable
22	R/W	0	ING_RATE_UNIT_6	0 = Bytes 1 = Packets
21	R/W	0	ING_CF_6	Coupling flag for ingress rate limit
20	R/W	0	ING_CM_6	Color mode for ingress rate limit

Table 5-320 PORT6_ING_RATE_CTRL1 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
19:18	R/W	01	ING_RATE_E_TIME_SLOT_6	Excess Ingress rate limit control timer slot. 00 = 100 μ s 01 = 1 ms 10 = 10 ms 11 = 100 ms Note: If port rate limit set to less than 96 kbps, do not select 100 μ s as time slot.
17:15	R/W	0	ING_EBS_6	Excess burst size for ingress rate limit
14:0	R/W	0x7FFF	ING_EIR_6	Excess Ingress rate limit for all priority. Rate is limited to times of 32 kbps. Default 15'h7FFF is for disable rate limit for ingress. If these bits are set to 15'h0, no frame is received in from this port.

5.7.168 PORT6_ING_RATE_CTRL2

Address offset: 0x0B68

Table 5-321 summarizes the port 6 ingress rate limit control 2 register.

Table 5-321 PORT6_ING_RATE_CTRL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	RESERVED	
15	R/W	0	ING_C_MULTI_RATE_EN_6	Ingress committed rate limit enable to count the multicast frames
14	R/W	0	ING_C_UNI_RATE_EN_6	Ingress committed rate limit enable to count the unicast frames
13	R/W	0	ING_C_UNK_MULTI_RATE_EN_6	Ingress committed rate limit enable to count the unknown multicast frames
12	R/W	0	ING_C_UNK_UNI_RATE_EN_6	Ingress committed rate limit enable to count the unknown unicast frames
11	R/W	0	ING_C_BROAD_RATE_EN_6	Ingress committed rate limit enable to count the broadcast frames
10	R/W	0	ING_C_MANAGE_RATE_EN_6	Ingress committed rate limit enable to count the management frames
9	R/W	0	ING_C_TCP_CTRL_RATE_EN_6	Ingress committed rate limit enable to count the TCP control frames
8	R/W	0	ING_C_ING_MIRROR_RATE_EN_6	Ingress committed rate limit enable to count the ingress mirror frames
7	R/W	0	ING_E_MULTI_RATE_EN_6	Ingress excess rate limit enable to count the multicast frames

Table 5-321 PORT6_ING_RATE_CTRL2 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
6	R/W	0	ING_E_UNI_RATE_EN_6	Ingress excess rate limit enable to count the unicast frames
5	R/W	0	ING_E_UNK_MULTI_RATE_EN_6	Ingress excess rate limit enable to count the unknown multicast frames
4	R/W	0	ING_E_UNK_UNI_RATE_EN_6	Ingress excess rate limit enable to count the unknown unicast frames
3	R/W	0	ING_E_BROAD_RATE_EN_6	Ingress excess rate limit enable to count the broadcast frames
2	R/W	0	ING_E_MANAGE_RATE_EN_6	Ingress excess rate limit enable to count the management frames
1	R/W	0	ING_E_TCP_CTRL_RATE_EN_6	Ingress excess rate limit enable to count the TCP control frames
0	R/W	0	ING_E_ING_MIRROR_RATE_EN_6	Ingress excess rate limit enable to count the ingress mirror frames

5.7.169 CPU_GROUP_CTRL

Address offset: 0x0B70

Table 5-322 summarizes the CPU packet remap priority control register.

Table 5-322 CPU_GROUP_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	CPU_GROUP_REMAP_EN	Remap the packet (to CPU) priority
30:23	RO	0	RESERVED	
22:20	R/W	0	CPU_GROUP5_PRI	Header type 5'h19–5'h1A
19	RO	0	RESERVED	
18:16	R/W	1	CPU_GROUP4_PRI	Header type 5'h17–5'h18
15	RO	0	RESERVED	
14:12	R/W	2	CPU_GROUP3_PRI	Header type 5'hE–5'h16
11	RO	0	RESERVED	
10:8	R/W	3	CPU_GROUP2_PRI	Header type 5'h5–5'hD
7	RO	0	RESERVED	
6:4	R/W	4	CPU_GROUP1_PRI	Header type 5'h3,5'h4
3	RO	0	RESERVED	
2:0	R/W	5	CPU_GROUP0_PRI	Header type 5'h1,5'h2,5'h1C

5.8 PKT edit register (offset range: 0x0C00–0x0C80)

Table 5-323 summarizes the packet editor registers.

Table 5-323 Packet editor register summary

Name	Offset range
PKT edit control register	0x0C00
Port0 queue remap register	0x0C40–0x0C44
Port1 queue remap register	0x0C48
Port2 queue remap register	0x0C4C
Port3 queue remap register	0x0C50
Port4 queue remap register	0x0C54
Port5 queue remap register	0x0C58–0x0C5C
Port6 queue remap register	0x0C60–0x0C64
Router default VID register	0x0C70–0x0C7C
Router egress VLAN mode register	0x0C80

5.8.1 PKT_EDIT_CTRL

Address offset: 0x0C00

Table 5-324 summarizes the PKT edit control register.

Table 5-324 PKT_EDIT_CTRL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:27	RO	0	RESERVED	
26	R/W	0	VLAN_PRI_REMAP_EN_6	1 = Frame sent out from port6; remap priority based on frame priority.
25	R/W	0	VLAN_PRI_REMAP_EN_5	1 = Frame sent out from port5; remap priority based on frame priority.
24	R/W	0	VLAN_PRI_REMAP_EN_4	1 = Frame sent out from port4; remap priority based on frame priority.
23	R/W	0	VLAN_PRI_REMAP_EN_3	1 = Frame sent out from port3; remap priority based on frame priority.
22	R/W	0	VLAN_PRI_REMAP_EN_2	1 = Frame sent out from port2; remap priority based on frame priority.
21	R/W	0	VLAN_PRI_REMAP_EN_1	1 = Frame sent out from port1; remap priority based on frame priority.
20	R/W	0	VLAN_PRI_REMAP_EN_0	1 = Frame sent out from port0; remap priority based on frame priority.
19:12	R/W	0	IP_TTL	

Table 5-324 PKT_EDIT_CTRL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
11	R/W	0	IP_TTL_CHANGE_EN	1 = Frame TTL change to IP_TTL.
10	R/W	0	IPV4_ID_RANDOM_EN	1 = Frame sent out with random ID.
9	R/W	0	IPV4_DF_CLEAR_EN	1 = IPv4 DF field cleared to zero.
8	RO	0	RESERVED	
7	RO	0	RESERVED	
6:2	RO	0	RESERVED	
1	R/W	0	TO_CPU_VID_CHG_EN	The VID option for the TO CPU frames. 0 = Keep original VID 1 = Change to internal VID
0	R/W	0	RM_RTD_PPPOE_EN	When packet is routed, and the PPPOE_CMD in ARP table is zero. 0 = Do nothing. 1 = Remove PPPoE header if the packet has PPPoE header.

5.8.2 PORT0_QUEUE_REMAP_REG0

Address offset: 0x0C40

Table 5-325 summarizes the port 0 queue remap register 0.

Table 5-325 PORT0_QUEUE_REMAP_REG0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	PORT0_QUEUE3_EN	Enable queue 3 remap
30:28	RO	0	RESERVED	
27:24	R/W	0	PORT0_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT0_QUEUE2_EN	Enable queue 2 remap
22:20	RO	0	RESERVED	
19:16	R/W	0	PORT0_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT0_QUEUE1_EN	Enable queue 1 remap
14:12	RO	0	RESERVED	
11:8	R/W	0	PORT0_QUEUE1_IDX	Queue 1 remap table index
7	R/W	0	PORT0_QUEUE0_EN	Enable queue 0 remap
6:4	RO	0	RESERVED	
3:0	R/W	0	PORT0_QUEUE0_IDX	Queue 0 remap table index

5.8.3 PORT0_QUEUE_REMAP_REG1

Address offset: 0x0C44

Table 5-326 summarizes the port 0 queue remap register 1.

Table 5-326 PORT0_QUEUE_REMAP_REG0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	RESERVED	
15	R/W	0	PORT0_QUEUE5_EN	Enable queue 5 remap
14:12	RO	0	RESERVED	
11:8	R/W	0	PORT0_QUEUE5_IDX	Queue 5 remap table index
7	R/W	0	PORT0_QUEUE4_EN	Enable queue 4 remap
6:4	RO	0	RESERVED	
3:0	R/W	0	PORT0_QUEUE4_IDX	Queue 4 remap table index

5.8.4 PORT1_QUEUE_REMAP_REG0

Address offset: 0x0C48

Table 5-327 summarizes the port 1 queue remap register 0.

Table 5-327 PORT1_QUEUE_REMAP_REG0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	PORT1_QUEUE3_EN	Enable queue 3 remap
30:28	RO	0	RESERVED	
27:24	R/W	0	PORT1_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT1_QUEUE2_EN	Enable queue 2 remap
22:20	RO	0	RESERVED	
19:16	R/W	0	PORT1_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT1_QUEUE1_EN	Enable queue 1 remap
14:12	RO	0	RESERVED	
11:8	R/W	0	PORT1_QUEUE1_IDX	Queue 1 remap table index
7	R/W	0	PORT1_QUEUE0_EN	Enable queue 0 remap
6:4	RO	0	RESERVED	
3:0	R/W	0	PORT1_QUEUE0_IDX	Queue 0 remap table index

5.8.5 PORT2_QUEUE_REMAP_REG0

Address offset: 0x0C4C

Table 5-328 summarizes the port 2 queue remap register 0.

Table 5-328 PORT2_QUEUE_REMAP_REG0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	PORT2_QUEUE3_EN	Enable queue 3 remap
30:28	RO	0	RESERVED	
27:24	R/W	0	PORT2_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT2_QUEUE2_EN	Enable queue 2 remap
22:20	RO	0	RESERVED	
19:16	R/W	0	PORT2_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT2_QUEUE1_EN	Enable queue 1 remap
14:12	RO	0	RESERVED	
11:8	R/W	0	PORT2_QUEUE1_IDX	Queue 1 remap table index
7	R/W	0	PORT2_QUEUE0_EN	Enable queue 0 remap
6:4	RO	0	RESERVED	
3:0	R/W	0	PORT2_QUEUE0_IDX	Queue 0 remap table index

5.8.6 PORT3_QUEUE_REMAP_REG0

Address offset: 0x0C50

Table 5-329 summarizes the port 3 queue remap register 0.

Table 5-329 PORT3_QUEUE_REMAP_REG0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	PORT3_QUEUE3_EN	Enable queue 3 remap
30:28	RO	0	RESERVED	
27:24	R/W	0	PORT3_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT3_QUEUE2_EN	Enable queue 2 remap
22:20	RO	0	RESERVED	
19:16	R/W	0	PORT3_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT3_QUEUE1_EN	Enable queue 1 remap
14:12	RO	0	RESERVED	
11:8	R/W	0	PORT3_QUEUE1_IDX	Queue 1 remap table index
7	R/W	0	PORT3_QUEUE0_EN	Enable queue 0 remap
6:4	RO	0	RESERVED	
3:0	R/W	0	PORT3_QUEUE0_IDX	Queue 0 remap table index

5.8.7 PORT4_QUEUE_REMAP_REG0

Address offset: 0x0C54

Table 5-330 summarizes the port 4 queue remap register 0.

Table 5-330 PORT4_QUEUE_REMAP_REG0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	PORT4_QUEUE3_EN	Enable queue 3 remap
30:28	RO	0	RESERVED	
27:24	R/W	0	PORT4_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT4_QUEUE2_EN	Enable queue 2 remap
22:20	RO	0	RESERVED	
19:16	R/W	0	PORT4_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT4_QUEUE1_EN	Enable queue 1 remap
14:12	RO	0	RESERVED	
11:8	R/W	0	PORT4_QUEUE1_IDX	Queue 1 remap table index
7	R/W	0	PORT4_QUEUE0_EN	Enable queue 0 remap
6:4	RO	0	RESERVED	
3:0	R/W	0	PORT4_QUEUE0_IDX	Queue 0 remap table index

5.8.8 PORT5_QUEUE_REMAP_REG0

Address offset: 0x0C58

Table 5-331 summarizes the port 5 queue remap register 0.

Table 5-331 PORT5_QUEUE_REMAP_REG0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	PORT5_QUEUE3_EN	Enable queue 3 remap
30:28	RO	0	RESERVED	
27:24	R/W	0	PORT5_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT5_QUEUE2_EN	Enable queue 2 remap
22:20	RO	0	RESERVED	
19:16	R/W	0	PORT5_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT5_QUEUE1_EN	Enable queue 1 remap
14:12	RO	0	RESERVED	
11:8	R/W	0	PORT5_QUEUE1_IDX	Queue 1 remap table index
7	R/W	0	PORT5_QUEUE0_EN	Enable queue 0 remap

Table 5-331 PORT5_QUEUE_REMAP_REG0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
6:4	RO	0	RESERVED	
3:0	R/W	0	PORT5_QUEUE0_IDX	Queue 0 remap table index

5.8.9 PORT5_QUEUE_REMAP_REG1

Address offset: 0x0C5C

Table 5-332 summarizes the port 5 queue remap register 1.

Table 5-332 PORT5_QUEUE_REMAP_REG1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	RESERVED	
15	R/W	0	PORT5_QUEUE5_EN	Enable queue 5 remap
14:12	RO	0	RESERVED	
11:8	R/W	0	PORT5_QUEUE5_IDX	Queue 5 remap table index
7	R/W	0	PORT5_QUEUE4_EN	Enable queue 4 remap
6:4	RO	0	RESERVED	
3:0	R/W	0	PORT5_QUEUE4_IDX	Queue 4 remap table index

5.8.10 PORT6_QUEUE_REMAP_REG0

Address offset: 0x0C60

Table 5-333 summarizes the port 6 queue remap register 0.

Table 5-333 PORT6_QUEUE_REMAP_REG0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	PORT6_QUEUE3_EN	Enable queue 3 remap
30:28	RO	0	RESERVED	
27:24	R/W	0	PORT6_QUEUE3_IDX	Queue 3 remap table index
23	R/W	0	PORT6_QUEUE2_EN	Enable queue 2 remap
22:20	RO	0	RESERVED	
19:16	R/W	0	PORT6_QUEUE2_IDX	Queue 2 remap table index
15	R/W	0	PORT6_QUEUE1_EN	Enable queue 1 remap
14:12	RO	0	RESERVED	

Table 5-333 PORT6_QUEUE_REMAP_REG0 bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
11:8	R/W	0	PORT6_QUEUE1_IDX	Queue 1 remap table index Enable queue 0 remap Queue 0 remap table index
7	R/W	0	PORT6_QUEUE0_EN	Enable queue 0 remap
6:4	RO	0	RESERVED	
3:0	R/W	0	PORT6_QUEUE0_IDX	Queue 0 remap table index

5.8.11 PORT6_QUEUE_REMAP_REG1

Address offset: 0x0C64

Table 5-334 summarizes the port 6 queue remap register 1.

Table 5-334 PORT6_QUEUE_REMAP_REG1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:16	RO	0	RESERVED	
15	R/W	0	PORT6_QUEUE5_EN	Enable queue 5 remap
14:12	RO	0	RESERVED	
11:8	R/W	0	PORT6_QUEUE5_IDX	Queue 5 remap table index
7	RO	0	PORT6_QUEUE4_EN	Enable queue 4 remap
6:4	RO	0	RESERVED	
3:0	R/W	0	PORT6_QUEUE4_IDX	Queue 4 remap table index

5.8.12 Router default VID register 0

Address offset: 0x0C70

Table 5-335 summarizes the router default VID register 0.

Table 5-335 Router default VID register 0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	RO	0	Reserved	
27:16	R/W	1	ROUTER_DEFAULT_VID1	Port 1 default VID for router
15:12	RO	0	Reserved	
11:0	R/W	1	ROUTER_DEFAULT_VID0	Port 0 default VID for router

5.8.13 Router default VID register 1

Address offset: 0x0C74

Table 5-336 summarizes the router default VID register 1.

Table 5-336 Router default VID register 1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	RO	0	Reserved	
27:16	R/W	1	ROUTER_DEFAULT_VID3	Port 3 default VID for router
15:12	RO	0	Reserved	
11:0	R/W	1	ROUTER_DEFAULT_VID2	Port 2 default VID for router

5.8.14 Router default VID register 2

Address offset: 0x0C78

Table 5-337 summarizes the router default VID register 2.

Table 5-337 Router default VID register 2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:28	RO	0	Reserved	
27:16	R/W	1	ROUTER_DEFAULT_VID5	Port 5 default VID for router
15:12	RO	0	Reserved	
11:0	R/W	1	ROUTER_DEFAULT_VID4	Port 4 default VID for router

5.8.15 Router default VID register 3

Address offset: 0x0C7C

Table 5-338 summarizes the router default VID register 3.

Table 5-338 Router default VID register 3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:12	RO	0	Reserved	
11:0	R/W	1	ROUTER_DEFAULT_VID6	Port 6 default VID for router

5.8.16 Router egress VLAN mode

Address offset: 0x0C80

Table 5-339 summarizes the router default VID register 3.

Table 5-339 Router egress VLAN mode bit description

Bits	R/W	Initial value	Mnemonic	Description
31:26	RO	0	RESERVED	
25:24	R/W	0	ROUTER_EG_VLAN_MODE6	Router egress VLAN mode of port 6
23:22	RO	0	RESERVED	
21:20	R/W	0	ROUTER_EG_VLAN_MODE5	Router egress VLAN mode of port 5
19:18	RO	0	RESERVED	
17:16	R/W	0	ROUTER_EG_VLAN_MODE4	Router egress VLAN mode of port 4
15:14	RO	0	RESERVED	
13:12	R/W	0	ROUTER_EG_VLAN_MODE3	Router egress VLAN mode of port 3
11:10	RO	0	RESERVED	
9:8	R/W	0	ROUTER_EG_VLAN_MODE2	Router egress VLAN mode of port 2
7:6	RO	0	RESERVED	
5:4	R/W	0	ROUTER_EG_VLAN_MODE1	Router egress VLAN mode of port 1
3:2	RO	0	RESERVED	
1:0	R/W	0	ROUTER_EG_VLAN_MODE0	Router egress VLAN mode of port 0 00 = Egress transmits frames unmodified 01 = Egress transmits frames without VLAN 10 = Egress transmits frames with VLAN 11 = Untouched

5.9 Layer 3 register (offset range: 0x0E00–0x0E98)

Table 5-340 summarizes the layer 3 registers.

Table 5-340 Layer 3 register summary

Name	Offset range
Host router control register	0x0E00
Host router port-based control register	0x0E04–0x0E0C
WCMP hash table register	0x0E10–0x0E1C
WCMP next hop table register	0x0E20–0x0E2C
ARP entry lock control register	0x0E30
ARP used account register	0x0E34
HNAT control register	0x0E38
NAPT entry lock control register	0x0E3C–0x0E40

Table 5-340 Layer 3 register summary (cont.)

Name	Offset range
NAPT used account register	0x0E44
Entry edit data register	0X0E80–0X0E98
Entry edit control register	0x0E58

5.9.1 HROUTER_CONTROL

Address offset: 0x0E00

Table 5-341 summarizes the host router control register.

Table 5-341 HROUTER_CONTROL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:20	RO	0	RESERVED	
19	R/W	0	ARP_LEARN_MODE	0 = Only learn ARP to router. 1 = Learn All ARP
18	R/W	0x1	ARP_OVERWRITE_EN	1 = Overwrite enable
17:16	R/W	0x3	GLOBAL_LOCK_TIME	0 = Disable 1 = 100 μ s 2 = 1 ms 3 = 10 ms When edit one entry, lock current entry for a period; For example overwrite session when auto learn, or CPU force to write one session
15:8	R/W	0x24	ARP_AGE_TIME	6s*N, 0 = ARP aging disable
7:4			WCMP_HASH_EN	WCMP hash key support one or more field from SIP/SP/DIP/DP, every field has individual control bit to enable/disable it; Bit[0]: SIP Bit[1]: SP Bit[2]: DIP Bit[3]: DP 0 = Disable 1 = Enable
3:2	RO	0	RESERVED	
1	R/W	0	ARP_AGE_MODE	0 = Normal age mode; 1 = Stop age when AGE_FLAG is 1;
0	R/W	0x1	ROUTER_EN	0 = Disable host routing 1 = Enable host routing

5.9.2 HROUTER_PBASED_CONTROL0

Address offset: 0x0E04

Table 5-342 summarizes the host router port-based control 0 register.

Table 5-342 HROUTER_PBASED_CONTROL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	RO	0	RESERVED	
20:0	R/W	0	ARP_SOURCE_CHECK_MODE	Source check mode for ARP 0. Disable 1. Check SMAC & SIP 2. Check SMAC & SIP & SP 3. Check SMAC & SIP & VID 4. Check SMAC & SIP & SP & VID Port-based control: Bits[2:0] for port 0 Bits[5:3] for port 1

5.9.3 HROUTER_PBASED_CONTROL1

Address offset: 0x0E08

Table 5-343 summarizes the host router port-based control 1 register.

Table 5-343 HROUTER_PBASED_CONTROL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:21	RO	0	RESERVED	
20:0	R/W	0	IP_SOURCE_CHECK_MODE	Source check mode for normal packet 0. Disable 1. Check SMAC & SIP 2. Check SMAC & SIP & SP 3. Check SMAC & SIP & VID 4. Check SMAC & SIP & SP & VID Port-based control Bits[2:0] for port 0 Bits[5:3] for port 1

5.9.4 HROUTER_PBASED_CONTROL2

Address offset: 0x0E0C

Table 5-344 summarizes the host router port-based control 2 register.

Table 5-344 HROUTER_PBASED_CONTROL2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:23	RO	0	RESERVED	
22:16	R/W	0x7f	IP_SP_UPDATE_EN	Source port update enable Can update only when IP+MAC+VID match ARP entry and no source check violation; Port-based control Bit[16] for port 0 Bit[17] for port 1
15	RO	0	RESERVED	
14:8	R/W	0	ARP_REP_LEARN_EN	ARP reply learn enable Port-based control Bit[8] for port 0 Bit[9] for port 1
7	RO	0	RESERVED	
6:0	R/W	0	ARP_REQ_LEARN_EN	ARP request learn enable Port-based control Bit[0] for port 0 Bit[1] for port 1

5.9.5 WCMP_HASH_TABLE0

Address offset: 0x0E10

Table 5-345 summarizes the WCMP hash table 0 register.

Table 5-345 WCMP_HASH_TABLE0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	0	WCMP_HASH_TABLE0	

5.9.6 WCMP_HASH_TABLE1

Address offset: 0x0E14

Table 5-346 summarizes the WCMP hash table 1 register.

Table 5-346 WCMP_HASH_TABLE1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	0	WCMP_HASH_TABLE1	

5.9.7 WCMP_HASH_TABLE2

Address offset: 0x0E18

[Table 5-347](#) summarizes the WCMP hash table 2 register.

Table 5-347 WCMP_HASH_TABLE2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	0	WCMP_HASH_TABLE2	

5.9.8 WCMP_HASH_TABLE3

Address offset: 0x0E1C

[Table 5-348](#) summarizes the WCMP hash table 3 register.

Table 5-348 WCMP_HASH_TABLE3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	0	WCMP_HASH_TABLE3	

5.9.9 WCMP_NHOP_TABLE0

Address offset: 0x0E20

[Table 5-349](#) summarizes the WCMP next hop table 0 register.

Table 5-349 WCMP_NHOP_TABLE0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	0	WCMP_NHOP_TABLE0	Bit[7]: Next hop0 valid Bits[6:0]: Next hop0 index Next hop 1–3 use the same rule; Every next hop use 8 bits; total 4 next hops for every 32 bits.

5.9.10 WCMP_NHOP_TABLE1

Address offset: 0x0E24

Table 5-350 summarizes the WCMP next hop table 1 register.

Table 5-350 WCMP_NHOP_TABLE1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	0	WCMP_NHOP_TABLE1	Bit[7]: Next hop0 valid Bits[6:0]: Next hop0 index Next hop 1–3 use the same rule; Every next hop use 8 bits; total 4 next hops for every 32 bits.

5.9.11 WCMP_NHOP_TABLE2

Address offset: 0x0E28

Table 5-351 summarizes the WCMP next hop table 2 register.

Table 5-351 WCMP_NHOP_TABLE2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	0	WCMP_NHOP_TABLE2	Bit[7]: Next hop0 valid Bits[6:0]: Next hop0 index Next hop 1–3 use the same rule; Every next hop use 8 bits; total 4 next hops for every 32 bits.

5.9.12 WCMP_NHOP_TABLE3

Address offset: 0x0E2C

Table 5-352 summarizes the WCMP next hop table 3 register.

Table 5-352 WCMP_NHOP_TABLE3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/W	0	WCMP_NHOP_TABLE3	Bit[7]: Next hop0 valid Bits[6:0]: Next hop0 index Next hop 1–3 use the same rule; Every next hop use 8 bits; total 4 next hops for every 32 bits.

5.9.13 ARP_ENTRY_LOCK_CONTROL

Address offset: 0x0E30

Table 5-353 summarizes the ARP entry lock control register.

Table 5-353 ARP_ENTRY_LOCK_CONTROL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	ARP_SW_LOCK_EN	When enabled, specific entry always locked by software; When disabled, LOCK_INDEX show locked entry by hardware itself.
30:11	RO	0	RESERVED	
10	RO	0	ARP_HW_LOCK_STATUS	When software lock disable, the HW_LOCK_STATUS shows the lock status by hardware;
9:7	RO	0	RESERVED	
6:0	R/WW	0	ARP_LOCK_INDEX	Depend: ARP_HW_LOCK_EN, arp_hw_lock_index[6:0], Entry index locked by software or hardware;

5.9.14 ARP_USED_ACCOUNT

Address offset: 0x0E34

Table 5-354 summarizes the ARP used account register.

Table 5-354 ARP_USED_ACCOUNT bit description

Bits	R/W	Initial value	Mnemonic	Description
31:8	RO	0	RESERVED	
7:0	RO	0	ARP_USED_CNT	Total used session in ARP table;

5.9.15 HNAT_CONTROL

Address offset: 0x0E38

Table 5-355 summarizes the HNAT control register.

Table 5-355 HNAT_CONTROL bit description

Bits	R/W	Initial value	Mnemonic	Description
31:23	RO	0	RESERVED	
22	R/W	0	NAPT_AGE_SPD_UP_STEP	0 = Double 1 = Quadruple To control the speed up degree, if set as 0, double the aging speed; if set as 1, quadruple the aging speed;
21:20	R/W	2	NAPT_AGE_SPD_UP_THRESH	0: Disable 1: 1/4 2: 1/8 3: 1/16 The ratio of the remaining entry number; when reach the ratio, aging scheme speeds up.
19:18	R/W	0	NAPT_UDP_AGE_STEP	0: 1 1: 2 2: 3 3: 4 To set the UDP aging step value
17:16	R/W	0	NAPT_TCP_AGE_STEP	0: 1 1: 2 2: 3 3: 4 To set the TCP aging step value, GRE share the same setting;
15:8	R/W	0xa	NAPT_AGE_TIMER	28sxN N = 0, aging disable. NAPT and GRE share the same age setting
7	R/W	0	NAPT_AGE_MODE	0 = Normal age mode; 1 = Stop age when NAPT AGE_FLAG is 1;
6:5	R/W	2	NAT_HASH_MODE	0: SP 1: SIP 2: SP+SIP 3: Reserved
4	R/W	1	NAPT_OVERWRITE_EN	0 = Cannot overwrite; 1 = When entry violation, new entry can overwrite old entry;
3:2	R/W	0	NAPT_MODE	0: Full cone mode 1: Strict cone mode 2: Port strict mode/symmetric mode 3: Reserved
1	R/W	1	HNAT_EN	Enable or disable basic NAT
0	R/W	1	HNAPT_EN	Enable or disable HNAPT

5.9.16 NAPT_ENTRY_LOCK_CONTROL0

Address offset: 0x0E3C

Table 5-356 summarizes the NAPT entry lock control 0 register.

Table 5-356 NAPT_ENTRY_LOCK_CONTROL0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	NAPT_SW_LOCK_EN0	When enabled, specific entry always locked by software; When disabled, LOCK_INDEX show locked entry by hardware itself.
30:11	RO	0	RESERVED	
10	RO	0	NAPT_HW_LOCK_STATUS0	When software lock disable, the HW_LOCK_STATUS shows the lock status by hardware;
9:0	R/WW	0	NAPT_LOCK_INDEX0	Depend: NAPT_HW_LOCK_EN0,NAPT_HW_LOCK_INDEX0[9:0], entry index locked by software or hardware.

5.9.17 NAPT_ENTRY_LOCK_CONTROL1

Address offset: 0x0E40

Table 5-357 summarizes the NAPT entry lock control 1 register.

Table 5-357 NAPT_ENTRY_LOCK_CONTROL1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/W	0	NAPT_SW_LOCK_EN1	When enabled, specific entry always locked by software; When disabled, LOCK_INDEX show locked entry by hardware itself.
30:11	RO	0	RESERVED	
10	RO	0	NAPT_HW_LOCK_STATUS1	When software lock disable, the HW_LOCK_STATUS shows the lock status by hardware;
9:0	R/WW	0	NAPT_LOCK_INDEX1	Depend: NAPT_HW_LOCK_EN1,NAPT_HW_LOCK_INDEX1[9:0], Entry index locked by software or hardware.

5.9.18 NAPT_USED_ACCOUNT

Address offset: 0x0E44

Table 5-358 summarizes the NAPT used account register.

Table 5-358 NAPT_USED_ACCOUNT bit description

Bits	R/W	Initial value	Mnemonic	Description
31:11	RO	0	RESERVED	
10:0	RO	0	NAPT_USED_CNT	Total used session in NAPT table

5.9.19 ENTRY_EDIT_DATA0

Address offset: 0x0E80

Table 5-359 summarizes the entry edit data 0 register.

Table 5-359 ENTRY_EDIT_DATA0 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ENTRY_EDIT_DATA0	Depend: cmd_complete, entry_data0_in[31:0]

5.9.20 ENTRY_EDIT_DATA1

Address offset: 0x0E84

Table 5-360 summarizes the entry edit data 1 register.

Table 5-360 ENTRY_EDIT_DATA1 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ENTRY_EDIT_DATA1	Depend: cmd_complete, entry_data1_in[31:0]

5.9.21 ENTRY_EDIT_DATA2

Address offset: 0x0E88

Table 5-361 summarizes the entry edit data 2 register.

Table 5-361 ENTRY_EDIT_DATA2 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ENTRY_EDIT_DATA2	Depend: cmd_complete, entry_data2_in[31:0]

5.9.22 ENTRY_EDIT_DATA3

Address offset: 0x0E8C

Table 5-362 summarizes the entry edit data 3 register.

Table 5-362 ENTRY_EDIT_DATA3 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ENTRY_EDIT_DATA3	Depend: cmd_complete, entry_data3_in[31:0]

5.9.23 ENTRY_EDIT_DATA4

Address offset: 0x0E90

Table 5-363 summarizes the entry edit data 4 register.

Table 5-363 ENTRY_EDIT_DATA4 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ENTRY_EDIT_DATA4	Depend: cmd_complete, entry_data4_in[31:0]

5.9.24 ENTRY_EDIT_DATA5

Address offset: 0x0E94

Table 5-364 summarizes the entry edit data 5 register.

Table 5-364 ENTRY_EDIT_DATA5 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ENTRY_EDIT_DATA5	Depend:cmd_complete,entry_data5_in[31:0]

5.9.25 ENTRY_EDIT_DATA6

Address offset: 0x0E98

Table 5-365 summarizes the entry edit data 6 register.

Table 5-365 ENTRY_EDIT_DATA6 bit description

Bits	R/W	Initial value	Mnemonic	Description
31:0	R/WW	0	ENTRY_EDIT_DATA6	Depend:cmd_complete,entry_data6_in[31:0]

5.9.26 ENTRY_EDIT_CONTROL

Address offset: 0x0E58

Table 5-366 summarizes the entry edit control register.

Table 5-366 ENTRY_EDIT_CONTROL bit description

Bits	R/W	Initial value	Mnemonic	Description
31	R/WSC	0	BUSY	Depend: CMD_COMPLETE, 0 = Hardware clear to indicate operation complete. 1 = Write 1 to start operation.
30:23	RO	0	RESERVED	
22	R/W	0	SPECIFIC_SP_EN	Enable specific source port for flush and get next command, valid for ARP table;
21	R/W	0	SPECIFIC_VID	Enable specific VID for flush and get next command, valid for ARP table;
20	R/W	0	SPECIFIC_PIP_EN	Enable specific public IP for flush and get next command, valid for NAPT table; If enabled, according tip index field is fill in for the command;
19	R/W	0	SPECIFIC_SIP_EN	Enable specific source IP for flush and get next command, valid for NAPT table;
18	R/W	0	SPECIFIC_AGE_EN	Enable specific age value for flush and get next command, valid for NAPT and ARP table; Use <= as compare way (and >0 is the implied condition)
17:8	R/WW	0	CMD_INDEX	For NAPT and ARP table, hardware returns entry index information for add one/delete one/search one/get next command.
7	RO	0	STATUS	Depend: CMD_COMPLETE
6	RO	0	RESERVED	
5:4	R/W	0	TABLE_SEL	0 = NAPT Table 1 = Reserved 2 = NAT Table 3 = ARP Table

Table 5-366 ENTRY_EDIT_CONTROL bit description (cont.)

Bits	R/W	Initial value	Mnemonic	Description
3	RO	0	RESERVED	
2:0	R/W	0	ENTRY_FUNC	0 = No action 1 = Flush entry 2 = Add one entry 3 = Delete one entry 4 = Get next valid entry, not valid for SIP table and NAT Table, 5 = Search one entry a. For NAPT and ARP table, fill in key for add one/delete one/search one; fill in the 5-tuple as search key (Private IP, Private Port Number, Public IP Public Port number, Protocol); for GRE entry (Private IP, Call ID, Public IP, Call ID, Protocol); for ARP table, fill in Destination IP as search key; b. For Flush and Get Next command if need extra condition, fill in related content to according field which defined in entry data structure, and set according enable control bit define in bits[22:18].

5.10 PHY control registers

Table 5-367 summarizes the PHY control registers.

Table 5-367 PHY control register summary

Offset (Hex)	Description	Page
0	Control register	page 321
1	Status register	page 322
2	PHY identifier	page 324
3	PHY identifier 2	page 324
4	Auto-negotiation advertisement register	page 325
5	Link partner ability register	page 327
6	Auto-negotiation expansion register	page 329
7	Next page transmit register	page 329
8	Link partner next page register	page 330
9	1000BASE-T control register	page 331
A	1000BASE-T status register	page 333
B	Reserved	
C	Reserved	
D	Reserved	
E	Reserved	

Table 5-367 PHY control register summary (cont.)

Offset (Hex)	Description	Page
F	Extended status register	page 335
10	PHY-specific control register	page 335
11	PHY-specific status register	page 336
12	Interrupt enable register	page 338
13	Interrupt status register	page 340
14	Extended PHY-specific register	page 341
15	Receive error counter register	page 342
16	Virtual cable tester control register	page 343
17	Reserved	
18	Reserved	
19	Reserved	
1A	Reserved	
1B	Reserved	
1C	Virtual cable tester status register	page 343
1D	Debug port 1 (address offset)	page 344
1E	Debug port 2 (data port)	page 344
1F	Reserved	

Table 5-368 summarizes the registers in MMD3 (MDIO manageable device address 3 for PCS).

Table 5-368 PHY control register summary — MMD3

Offset (Hex)	Description	Page
0	PCS control register	page 352
1	PCS status register	page 352
E	EEE capability	page 353
16	EEE wake error counter	page 354

Table 5-369 summarizes the registers in MMD7 (MDIO manageable device address 7 for PCS).

Table 5-369 PHY control register summary — MMD7

Offset	Description	Page
0	AN control	page 354
1	AN status	page 355
5	AN package register	page 355
2	AN XNP transmit	page 356

Table 5-369 PHY control register summary — MMD7 (cont.)

Offset	Description	Page
17	AN XNP transmit1	page 356
18	AN XNP transmit2	page 356
19	ANXNP ability	page 357
1A	ANXNP ability1	page 357
1B	ANXNP ability2	page 357
3C	EEE advertisement	page 358
3D	EEE LP advertisement	page 358
8000	EEE ability auto-negotiation result	page 359

5.10.1 Control register

Address offset: 0x00

Table 5-370 summarizes the control registers.

Table 5-370 Control register bit description

Bits	Symbol	Type	Description	
15	Reset	Mode	R/W	PHY Software Reset. Writing a 1 to this bit causes the PHY the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 0 = Normal operation 1 = PHY reset
		HW Rst	0	
		SW Rst	SC	
14	Loopback	Mode	R/W	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. 0 = Disable loopback 1 = Enable loopback
		HW Rst	0	
		SW Rst	0	
13	Speed Selection	Mode	R/W	11 = Reserved 10 = 1000 Mb/s 01 = 100 Mb/s 00 = 10 Mb/s
		HW Rst		
		SW Rst		
12	Auto-negotiation	Mode	R/W	0 = Disable auto-negotiation process 1 = Enable auto-negotiation process
		HW Rst		
		SW Rst		
11	Power Down	Mode	R/W	When the port is switched from power down to normal operation, software reset and restart auto-negotiation are performed even when bits reset (bit[15]) and restart auto-negotiation (bit[9]) are not set by the user. 0 = Normal operation 1 = Power down
		HW Rst	0	
		SW Rst	0	

Table 5-370 Control register bit description (cont.)

Bits	Symbol	Type		Description
10	Isolate	Mode	R/W	The GMII/MII output pins are tristated when this bit is set to 1. The GMII/MII inputs are ignored. 0 = Normal operation 1 = Isolate
		HW Rst	0	
		SW Rst	0	
9	Restart Auto-negotiation	Mode	R/W, SC	Auto-negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (bit[9]) is set. 0 = Normal operation 1 = Restart auto-negotiation process
		HW Rst	0	
		SW Rst	SC	
8	Duplex Mode	Mode	R/W, SC	0 = Half-duplex 1 = Full-duplex
		HW Rst		
		SW Rst		
7	Collision Test	Mode	R/W	Setting this bit to 1 causes the COL pin to assert whenever the TX_EN pin is asserted. 0 = Disable COL signal test 1 = Enable COL signal test
		HW Rst	0	
		SW Rst	0	
6	Speed Selection (MSB)	Mode	R/W	See bit[13]
		HW Rst	See Desc.	
		SW Rst		
5:0	Reserved	Mode	RO	Always be 00000.
		HW Rst	000000	
		SW Rst	00000	

5.10.2 Status Register

Address offset: 0x01, or 0d01

Table 5-371 summarizes the status registers.

Table 5-371 Status registers bit description

Bits	Symbol	Type		Description
15	100BASE-T4	Mode	RO	100BASE-T4 This protocol is not available. 0 = PHY not able to perform 100BASE-T4
		HW Rst	Always 0	
		SW Rst	Always 0	
14	100BASE-X Full	Mode	RO	Capable of 100BASE-Tx full-duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	

Table 5-371 Status registers bit description (cont.)

Bits	Symbol	Type		Description
13	100BASE-X Half	Mode	RO	Capable of 100BASE-Tx half-duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
12	10 Mbps Full-Duplex	Mode	RO	Capable of 10BASE-Te full duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
11	10 Mbps Half-Duplex	Mode	RO	Capable of 10 Mbps half duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
10	100BASE-T2 Full-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst	Always 0	
		SW Rst	Always 0	
9	100BASE-T2 Half-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst	Always 0	
		SW Rst	Always 0	
8	Extended Status	Mode	RO	Extended status information in the extended status register
		HW Rst	Always 0	
		SW Rst	Always 0	
7	Reserved	Mode	RO	Always be 0.
		HW Rst	Always 0	
		SW Rst	Always 0	
6	MF Preamble Suppression	Mode	RO	PHY accepts management frames with preamble suppressed
		HW Rst	Always 1	
		SW Rst	Always 1	
5	Auto-negotiation Complete	Mode	RO	0 = Auto-negotiation process incomplete 1 = Auto-negotiation process complete
		HW Rst	0	
		SW Rst	0	
4	Remote Fault	Mode	RO, LH	0 = Remote fault condition not detected 1 = Remote fault condition detected
		HW Rst	0	
		SW Rst	0	
3	Auto-negotiation Ability	Mode	RO	1 = PHY able to perform auto-negotiation
		HW Rst	Always 1	
		SW Rst	Always 1	

Table 5-371 Status registers bit description (cont.)

Bits	Symbol	Type		Description
2	Link Status	Mode	RO, LL	This register bit indicates whether the link was lost since the last read. For the current link status, read bit[10] of PHY-specific status register. 0 = Link is down 1 = Link is up
		HW Rst	0	
		SW Rst	0	
1	Jabber Detect	Mode	RO, LH	0 = Jabber condition not detected 1 = Jabber condition detected
		HW Rst	0	
		SW Rst	0	
0	Extended Capability	Mode	RO	1 = Extended register capabilities
		HW Rst	Always 1	
		SW Rst	Always 1	

5.10.3 PHY identifier

Address offset: 0x02 or 0d02

Table 5-372 summarizes the PHY identifier.

Table 5-372 PHY Identifier bit description

Bits	Symbol	Type		Description
15:0	ONI[18:3]	Mode	RO	Organizationally unique identifier bits[18:3]
		HW Rst	Always 16'h004d	
		SW Rst	Always 16'h004d	

5.10.4 PHY Identifier 2

Address offset: 0x3

Table 5-373 summarizes the PHY identifiers 2.

Table 5-373 PHY Identifier 2 bit description

Bits	Symbol	Type		Description
15:10	ONI[24:19]	Mode	RO	Organizationally unique identifier bits[24:19]
		HW Rst	Always 16'hd033	
9:4	Manufacturer's Model Number	SW Rst	Always 16'hd033	
3:0	Revision Number			

5.10.5 Auto-negotiation advertisement register

Address offset: 0x04, or 0d04

Table 5-374 summarizes the auto-negotiation advertisement register.

Table 5-374 Auto-negotiation advertisement register bit description

Bits	Symbol	Type		Description
15	Next Page	Mode	R/W	<p>The value of this bit is updated immediately after writing this register, but the value written to this bit does not take effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (control register bit[15]) ■ Restart auto-negotiation is asserted (control register bit[9]) ■ Power down (control register bit[11]) transitions from power down to normal operation ■ Link goes down <p>If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register is set to 0 if no additional next pages are needed.</p> <p>0 = Not advertised 1 = Advertise</p>
		HW Rst	0	
		SW Rst	Update	
14	ACK	Mode	RO	Must be 0.
		HW Rst	Always 0	
		SW Rst	Always 0	
13	Remote Fault	Mode	R/W	<p>0 = Do not set remote fault bit 1 = Set remote fault bit</p>
		HW Rst	Always 0	
		SW Rst	Always 0	
12	Reserved	Mode	RO	Always 0.
		HW Rst	Always 0	
		SW Rst	Always 0	
11	Asymmetric Pause	Mode	R/W	<p>The value of this bit is updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (control register bit[15]) ■ Restart auto-negotiation is asserted (control register bit[9]) ■ Power down (control register bit[11]) transitions from power down to normal operation ■ Link goes down <p>0 = No asymmetric pause 1 = Asymmetric pause</p> <p>Note: This bit has added the pad control and can be set from the F001 top. Its default value is one.</p>
		HW Rst	1	
		SW Rst	Update	

Table 5-374 Auto-negotiation advertisement register bit description (cont.)

Bits	Symbol	Type		Description
10	PAUSE	Mode	R/W	<p>The value of this bit is updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (control register bit[15]) ■ Restart auto-negotiation is asserted (control register bit[9]) ■ Power down (control register bit[11]) transitions from power down to normal operation ■ Link goes down <p>0 = MAC PAUSE not implemented 1 = MAC PAUSE implemented</p> <p>Note: This bit has added the pad control and can be set from the F001 top, its default value is one.</p>
		HW Rst	1	
		SW Rst	Update	
9	100BASE-T4	Mode	RO	Not able to perform 100BASE-T4
		HW Rst	Always 0	
		SW Rst	Always 0	
8	100BASE-Tx	Mode	R/W	<p>The value of this bit is updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (control register bit[15]) ■ Restart auto-negotiation is asserted (control register bit[9]) ■ Power down (control register bit[11]) transitions from power down to normal operation ■ Link goes down <p>0 = Not advertised 1 = Advertise</p>
		HW Rst	1	
		SW Rst	Update	
7	100BASE-Tx Half Duplex	Mode	R/W	<p>The value of this bit is updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (control register bit[15]) ■ Restart auto-negotiation is asserted (control register bit[9]) ■ Power down (control register bit[11]) transitions from power down to normal operation ■ Link goes down <p>0 = Not advertised 1 = Advertise</p>
		HW Rst	1	
		SW Rst	Update	

Table 5-374 Auto-negotiation advertisement register bit description (cont.)

Bits	Symbol	Type		Description
6	10BASE-Te Full Duplex	Mode	R/W	The value of this bit is updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs: <ul style="list-style-type: none"> Software reset is asserted (control register bit[15]) Restart auto-negotiation is asserted (control register bit[9]) Power down (control register bit[11]) transitions from power down to normal operation Link goes down 0 = Not advertised 1 = Advertise
		HW Rst	1	
		SW Rst	Update	
5	10BASE-Te Half Duplex	Mode	R/W	The value of this bit is updated immediately after writing this register. But the value written to this bit does not take effect until any one of the following occurs: <ul style="list-style-type: none"> Software reset is asserted (control register bit[15]) Restart auto-negotiation is asserted (control register bit[9]) Power down (control register bit[11]) transitions from power down to normal operation Link goes down 0 = Not advertised 1 = Advertise
		HW Rst	1	
		SW Rst	Update	
4:0	Selector Field	Mode	RO	Selector field mode 00001 = 802.3
		HW Rst	Always 00001	
		SW Rst	Always 00001	

5.10.6 Link partner ability register

Address offset: 0x05, or 0d05

Table 5-375 summarizes the link partner ability register.

Table 5-375 Link partner ability bit description

Bits	Symbol	Type		Description
15	Next Page	Mode	RO	Received code word bit[15] 0 = Link partner not capable of next page 1 = Link partner capable of next page
		HW Rst	0	
		SW Rst	0	
14	ACK	Mode	RO	Acknowledge Received code word bit[14] 0 = Link partner does not have next page ability 1 = Link partner received link code word
		HW Rst	0	
		SW Rst	0	

Table 5-375 Link partner ability bit description (cont.)

Bits	Symbol	Type		Description
13	Remote Fault	Mode	RO	Remote fault
		HW Rst	0	Received code word bit[13]
		SW Rst	0	0 = Link partner has not detected remote fault 1 = Link partner detected remote fault
12	Reserved	Mode	RO	Technology ability field
		HW Rst	0	Received code word bit[12]
		SW Rst	0	
11	Asymmetric Pause	Mode	RO	Technology ability field
		HW Rst	0	Received code word bit[11]
		SW Rst	0	0 = Link partner does not request asymmetric pause 1 = Link partner requests asymmetric pause
10	PAUSE	Mode	RO	Technology ability field
		HW Rst	0	Received code word bit[0]
		SW Rst	0	0 = Link partner is not capable of pause operation 1 = Link partner is capable of pause operation
9	100BASE-T4	Mode		Technology ability field
		HW Rst		Received code word bit[9]
		SW Rst		0 = Link partner is not 100BASE-T4 capable 1 = Link partner is 100BASE-T4 capable
8	100BASE-Tx Full Duplex	Mode	RO	Technology ability field
		HW Rst	0	Received code word bit[8]
		SW Rst	0	0 = Link partner is not 100BASE-Tx full-duplex capable 1 = Link partner is 100BASE-Tx full-duplex capable
7	100BASE-Tx Half Duplex	Mode	RO	Technology ability field
		HW Rst	0	Received code word bit[7]
		SW Rst	0	0 = Link partner is not 100Base-TX half-duplex capable 1 = Link partner is 100BASE-Tx half-duplex capable
6	10BASE-Te Full Duplex	Mode	RO	Technology ability field
		HW Rst	0	Received code word bit[6]
		SW Rst	0	0 = Link partner is not 10BASE-Te full-duplex capable 1 = Link partner is 10BASE-Te full-duplex capable
5	10BASE-Te Half Duplex	Mode	RO	Technology ability field
		HW Rst	0	Received code word bit[5]
		SW Rst	0	0 = Link partner is not 10BASE-Te half-duplex capable 1 = Link partner is 10BASE-Te half-duplex capable
4:0	Selector field	Mode	RO	Selector field
		HW Rst	00000	Received code word bits[4:0]
		SW Rst	00000	

5.10.7 Auto-negotiation expansion register

Address offset: 0x06, or 0d06

Table 5-376 summarizes the auto-negotiation expansion register.

Table 5-376 Auto-negotiation expansion bit description

Bits	Symbol	Type		Description
15:5	Reserved	Mode	RO	Reserved. Must be 0.
		HW Rst	Always 0x000	
		SW Rst	Always 0x000	
4	Parallel Detection Fault	Mode	RO, LH	0 = No fault has been detected 1 = A fault has been detect
		HW Rst	0	
		SW Rst	0	
3	Link Partner Next Page Able	Mode	RO	0 = Link partner is not next page able 1 = Link partner is Next page able
		HW Rst	0	
		SW Rst	0	
2	Local Next Page Able	Mode	R/W	1 = Local device is next page able
		HW Rst	1	
		SW Rst	1	
1	Page Received	Mode	RO, LH	0 = No new page has been received 1 = A new page has been received
		HW Rst	0	
		SW Rst	0	
0	Link Partner Auto-negotiation Able	Mode	RO	0 = Link partner is not auto-negotiation enable 1 = Link partner is auto-negotiation enable
		HW Rst	0	
		SW Rst	0	

5.10.8 Next page transmit register

Address offset: 0x07, or 0d07

Table 5-377 summarizes the next page transmit register.

Table 5-377 Next page transmit register bit description

Bits	Symbol	Type		Description
15	Next Page	Mode	R/W	Transmit code word bit[15]
		HW Rst	0	
		SW Rst	0	

Table 5-377 Next page transmit register bit description (cont.)

Bits	Symbol	Type		Description
14	Reserved	Mode	R/W	Transmit code word bit[14]
		HW Rst	0	
		SW Rst	0	
13	Message Page Mode	Mode	R/W	Transmit code word bit[13]
		HW Rst	0	
		SW Rst	0	
12	ACK	Mode	R/W	Transmit code word bit[12]
		HW Rst	0	
		SW Rst	0	
11	Toggle	Mode	RO	Transmit code word bit[11]
		HW Rst	0	
		SW Rst	0	
10:0	Message/Unformatted Field	Mode	R/W	Transmit code word bits[10:0]
		HW Rst	0x001	
		SW Rst	0x001	

5.10.9 Link partner next page register

Address offset: 0x08, or 0d08

Table 5-378 summarizes the link partner next page register.

Table 5-378 link partner next page bit description

Bits	Symbol	Type		Description
15	Next Page	Mode	RO	Transmit code word bit[15]
		HW Rst	0	
		SW Rst	0	
14	Reserved	Mode	RO	Transmit code word bit[14]
		HW Rst	0	
		SW Rst	0	
13	Message Page Mode	Mode	RO	Transmit code word bit[13]
		HW Rst	0	
		SW Rst	0	
12	Ack2	Mode	RO	Transmit code word bit[12]
		HW Rst	0	
		SW Rst	0	

Table 5-378 link partner next page bit description (cont.)

Bits	Symbol	Type		Description
11	Toggle	Mode	RO	Transmit code word bit[11]
		HW Rst	0	
		SW Rst	0	
10:0	Message/Unformatted Field	Mode	R/W	Transmit code word bits[10:0]
		HW Rst	0x000	
		SW Rst	0x000	

5.10.10 1000BASE-T control register

Address offset: 0x09, or 0d09

Table 5-379 summarizes the 1000BASE-T control register.

Table 5-379 1000BASE-T control bit description

Bits	Symbol	Type		Description
15:13	Test Mode	Mode	R/W	TX_TCLK comes from the RX_CLK pin for jitter testing in test modes 2 and 3. After exiting the test mode, hardware reset or software reset (control register bit[15]) is issued to ensure normal operation. 000 = Normal mode 001 = Test mode 1 — Transmit waveform test 010 = Test mode 2 — Transmit jitter test (master mode) 011 = Test mode 3 — Transmit jitter test (slave mode) 100 = Test mode 4 — Transmit distortion test 101, 110, 111 = Reserved
		HW Rst	000	
		SW Rst	Retain	
12	Master/Slave Manual Configuration Enable	Mode	R/W	The value of this bit is updated immediately after writing this register, but the value written to this bit does not take effect until any one of the following occurs: <ul style="list-style-type: none"> ■ Software reset is asserted (control register bit[15]) ■ Restart auto-negotiation is asserted (control register bit[9]) ■ Power down (control register bit[11]) transitions from power down to normal operation ■ Link goes down 0 = Automatic master/slave configuration 1 = Manual master/slave configuration
		HW Rst	0	
		SW Rst	Update	

Table 5-379 1000BASE-T control bit description (cont.)

Bits	Symbol	Type		Description
11	Master/Slave Configuration	Mode	R/W	<p>The value of this bit is updated immediately after writing this register, but the value written to this bit does not takes effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (control register bit[15]) ■ Restart auto-negotiation is asserted (control register bit[9]) ■ Power down (control register bit[11]) transitions from power down to normal operation ■ Link goes down <p>Bit[11] is ignored if bit[12] is equal to 0. 0 = Manual configure as slave 1 = Manual configure as master</p>
		HW Rst	0	
		SW Rst	Update	
10	Port Type	Mode	R/W	<p>The value of this bit is updated immediately after writing this register, but the value written to this bit does not takes effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (control register bit[15]) ■ Restart auto-negotiation is asserted (control register bit[9]) ■ Power down (control register bit[11]) transitions from power down to normal operation ■ Link goes down <p>Bit[10] is ignored if bit[12] is equal to 1. 0 = Prefer single port device (slave) 1 = Prefer multi-port device (master)</p>
		HW Rst	0	
		SW Rst	Update	
9	1000BASE-T Full Duplex	Mode	R/W	<p>The value of this bit is updated immediately after writing this register, but the value written to this bit does not takes effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (control register bit[15]) ■ Restart auto-negotiation is asserted (control register bit[9]) ■ Power down (control register bit[11]) transitions from power down to normal operation ■ Link goes down <p>0 = Not advertised 1 = Advertised</p>
		HW Rst	1	
		SW Rst	Update	
8	1000BASE-T Half-Duplex	Mode	R/W	<p>The value of this bit is updated immediately after writing this register, but the value written to this bit does not takes effect until any one of the following occurs:</p> <ul style="list-style-type: none"> ■ Software reset is asserted (control register bit[15]) ■ Restart auto-negotiation is asserted (control register bit[9]) ■ Power down (control register bit[11]) transitions from power down to normal operation ■ Link goes down <p>0 = Not advertised 1 = Advertised</p> <p>Note: The default setting is no 1000 base/half duplex advertised.</p>
		HW Rst	0	
		SW Rst	Update	

Table 5-379 1000BASE-T control bit description (cont.)

Bits	Symbol	Type		Description
		Mode	R/W	
7:0	Reserved	Mode	R/W	
		HW Rst	0	
		SW Rst	0	

5.10.11 1000BASE-T status register

Address offset: 0x0A, or 0d10

Table 5-380 summarizes the 1000BASE-T status register.

Table 5-380 1000BASE-T status bit description

Bits	Symbol	Type		Description
		Mode	R/W	
15	Master/Slave Configuration Fault	Mode	RO, LH	This register bit is cleared on read 0 = No fault detected 1 = Master/slave configuration fault detected
		HW Rst	0	
		SW Rst	0	
14	Master/Slave Configuration Resolution	Mode	RO	This register bit is not valid until bit[1] of the auto-negotiation expansion register is 1. 0 = Local PHY configuration resolved to slave 1 = Local PHY configuration resolved to master
		HW Rst	0	
		SW Rst	0	
13	Local Receiver Status	Mode	RO	0 = Local receiver is not ok 1 = Local receiver is ok
		HW Rst	0	
		SW Rst	0	
12	Remote Receiver Status	Mode	RO	0 = Remote receiver is not ok 1 = Remote receiver is ok
		HW Rst	0	
		SW Rst	0	
11	Link Partner 1000BASE-T Full Duplex Capability	Mode	RO	This register bit is not valid until bit[0] of the auto-negotiation expansion register is 1. 0 = Link Partner is not capable of 1000BASE-T half duplex 1 = Link Partner is capable of 1000BASE-T half duplex
		HW Rst	0	
		SW Rst	0	
10	Link Partner 1000BASE-T Half Duplex Capability	Mode	RO	This register bit is not valid until bit[0] of the auto-negotiation expansion register is 1. 0 = Link Partner is not capable of 1000BASE-T full duplex 1 = Link Partner is capable of 1000BASE-T full duplex
		HW Rst	0	
		SW Rst	0	
9:8	Reserved	Mode	RO	
		HW Rst	Always 0	
		SW Rst	Always 0	

Table 5-380 1000BASE-T status bit description (cont.)

Bits	Symbol	Type		Description
7:0	Idle Error Count	Mode	RO, SC	MSB of idle error counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and does not roll over.
		HW Rst	0	
		SW Rst	0	

5.10.12 MMD access control register

Address offset: 0x0D, or 0d13

Table 5-381 summarizes the MMD access control register.

Table 5-381 MMD access control bit description

Bits	Symbol	Type		Description
15:14	Function	Mode	R/W	00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only
		HW Rst.	00	
		SW Rst.	Retain	
13:5	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
4:0	DEVAD	Mode	R/W	Device address
		HW Rst.	0	
		SW Rst.	Update	

5.10.13 MMD access address data register

Address offset: 0x0E, or 0d14

Table 5-382 summarizes the MMD access address data register.

Table 5-382 MMD access address data register bit description

Bits	Symbol	Type		Description
15:0	Address Data	Mode	R/W	If bits[15:14] of the MMD access control register is 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register.
		HW Rst.	00	
		SW Rst.	Retain	

5.10.14 Extended status register

Address offset: 0x0F, or 0d15

Table 5-383 summarizes the extended status register.

Table 5-383 Extended status register bit description

Bits	Symbol	Type		Description
15	1000BASE-X Full Duplex	Mode	RO	PHY not able to perform 1000BASE-X full duplex
		HW Rst	Always 0	
		SW Rst	Always 0	
14	1000BASE-X Half Duplex	Mode	RO	PHY not able to perform 1000BASE-X half duplex
		HW Rst	Always 0	
		SW Rst	Always 0	
13	1000BASE-T Full-Duplex	Mode	RO	PHY able to perform 1000BASE-T full duplex
		HW Rst	Always 1	
		SW Rst	Always 1	
12	1000BASE-T Half-Duplex	Mode	RO	PHY not able to perform 1000BASE-T half duplex
		HW Rst	Always 0	
		SW Rst	Always 0	
11:0	Reserved	Mode	RO	
		HW Rst	Always 0	
		SW Rst	Always 0	

5.10.15 Function control register

Address offset: 0x10, or 0d16

Table 5-384 summarizes the function control register.

Table 5-384 Function control register bit description

Bits	Symbol	Type		Description
15:12	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
11	Assert CRS on Transmit	Mode	R/W	This bit has effect only in 10BASE-Te half-duplex mode: 0 = Assert on receiving. Do not assert on transmitting 1 = Assert on transmitting or receiving
		HW Rst	0	
		SW Rst	Retain	
10	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	

Table 5-384 Function control register bit description (cont.)

Bits	Symbol	Type		Description
9:8	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
6:5	MDI Crossover Mode	Mode	R/W	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
		HW Rst	11	
		SW Rst	Update	
4:3	Reserved	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
2	SQE Test	Mode	R/W	SQE test is automatically disabled in full-duplex mode. 0 = SQE test disabled 1 = SQE test enabled
		HW Rst	0	
		SW Rst	Retain	
1	Polarity Reversal	Mode	R/W	If polarity is disabled, then the polarity is forced to be normal in 10BASE-Te. 0 = Polarity reversal enabled 1 = Polarity reversal disabled
		HW Rst	0	
		SW Rst	Retain	
0	Disable Jabber	Mode	R/W	Jabber has effect only in 10BASE-Te half-duplex mode. 0 = Enable jabber function 1 = Disable jabber function
		HW Rst	0	
		SW Rst	Retain	

5.10.16 PHY-specific status register

Address offset: 0x11, or 0d17

Table 5-385 summarizes the PHY-specific status register.

Table 5-385 PHY-specific status register bit description

Bits	Symbol	Type		Description
15:14	Speed	Mode	RO	These status bits are valid when auto-negotiation is completed or auto-negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
		HW Rst	00	
		SW Rst	Retain	

Table 5-385 PHY-specific status register bit description (cont.)

Bits	Symbol	Type		Description
13	Duplex	Mode	RO	This status bit is valid only when auto-negotiation is complete or disabled. 0 = Half-duplex 1 = Full-duplex
		HW Rst	0	
		SW Rst	Retain	
12	Page Received (Real Time)	Mode	RO	0 = Page not received 1 = Page received
		HW Rst	0	
		SW Rst	Retain	
11	Speed and Duplex Resolved	Mode	RO	When auto-negotiation is not enabled for force speed mode. 0 = Not resolved 1 = Resolved
		HW Rst	0	
		SW Rst	0	
10	Link (Real Time)	Mode	RO	0 = Link down 1 = Link up
		HW Rst	0	
		SW Rst	0	
9:7	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
6	MDI Crossover Status	Mode	RO	This status bit is valid only when auto-negotiation is completed or auto-negotiation is disabled. 0 = MDI 1 = MDIX
		HW Rst	0	
		SW Rst	Retain	
5	Wirespeed downgrade	Mode	RO	0 = Not downgrade 1 = Downgrade
		HW Rst	0	
		SW Rst	0	
4	Reserved	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
3	Transmit Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only when auto-negotiation is completed or auto-negotiation is disabled. 0 = Transmit pause disabled 1 = Transmit pause enabled
		HW Rst	0	
		SW Rst	0	
2	Receive Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only when auto-negotiation is completed or auto-negotiation is disabled. 0 = Receive pause disabled 1 = Receive pause enabled
		HW Rst	0	
		SW Rst	Retain	

Table 5-385 PHY-specific status register bit description (cont.)

Bits	Symbol	Type		Description
1	Polarity (Real Time)	Mode	RO	0 = Normal 1 = Reversed
		HW Rst	0	
		SW Rst	0	
0	Jabber (Real Time)	Mode	RO	0 = No jabber 1 = Jabber
		HW Rst	0	
		SW Rst	Retain	

5.10.17 Interrupt enable register

Address offset: 0x12, or 0d18

Table 5-386 summarizes the interrupt enable register.

Table 5-386 Interrupt enable register bit description

Bits	Symbol	Type		Description
15	Auto-negotiation Error Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
14	Speed Changed Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
13	Duplex Changed Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
12	Page Received Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
11	Auto-negotiation Completed Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
10	Link Status Changed Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
9	Symbol Error Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	

Table 5-386 Interrupt enable register bit description (cont.)

Bits	Symbol	Type		Description
8	False Carrier Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
7	FIFO Over/Underflow Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
6	MDI Crossover Changed Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
5	Wirespeed-downgrade Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
4	Energy Detect Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
3:2	Reserved	Mode	R/W	Always 00.
		HW Rst	0	
		SW Rst	Retain	
1	Polarity Changed Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	
0	Jabber Interrupt Enable	Mode	R/W	0 = Interrupt disable 1 = Interrupt enable
		HW Rst	0	
		SW Rst	Retain	

5.10.18 Interrupt status register

Address offset: 0x13, or 0d19

Table 5-387 summarizes the interrupt status register.

Table 5-387 Interrupt status register bit description

Bits	Symbol	Type		Description
15	Auto-negotiation Error	Mode	RO, LH	An error occurs if master/slave does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 0 = No auto-negotiation error 1 = Auto-negotiation error
		HW Rst	0	
		SW Rst	Retain	
14	Speed Changed	Mode	RO, LH	0 = Speed not changed 1 = Speed changed
		HW Rst	0	
		SW Rst	Retain	
13	Reserved	Mode	RO, LH	Reserved
		HW Rst	0	
		SW Rst	Retain	
12	Page Received	Mode	RO	0 = Page not received 1 = Page received
		HW Rst	0	
		SW Rst	Retain	
11	Auto-negotiation Completed	Mode	RO	0 = Auto-negotiation incomplete 1 = Auto-negotiation complete
		HW Rst	0	
		SW Rst	Retain	
10	Link Status Changed	Mode	RO, LH	0 = Link status not changed 1 = Link status changed
		HW Rst	0	
		SW Rst	Retain	
9	Symbol Error	Mode	RO, LH	0 = No symbol error 1 = Symbol error
		HW Rst	0	
		SW Rst	Retain	
8	False Carrier	Mode	RO, LH	0 = No false carrier 1 = False carrier
		HW Rst	0	
		SW Rst	Retain	
7	FIFO Over/Underflow	Mode	RO, LH	0 = No FIFO error 1 = Over/underflow error Not implement, always 0.
		HW Rst	0	
		SW Rst	Retain	
6	MDI Crossover Changed	Mode	RO, LH	0 = Crossover not changed 1 = Crossover changed
		HW Rst	0	
		SW Rst	Retain	
5	Wirespeed-downgrade Interrupt	Mode	RO, LH	0 = No wirespeed-downgrade 1 = Wirespeed-downgrade detected.
		HW Rst	0	
		SW Rst	Retain	

Table 5-387 Interrupt status register bit description (cont.)

Bits	Symbol	Type		Description
4	Energy Detect Changed	Mode	RO, LH	0 = No energy detect state change detected 1 = Energy detect state changed Not implement, always 0.
		HW Rst	0	
		SW Rst	Retain	
3:2	Reserved	Mode	RO, LH	Always 0.
		HW Rst	0	
		SW Rst	Retain	
1	Polarity Changed	Mode	RO, LH	0 = Polarity not changed 1 = Polarity changed
		HW Rst	0	
		SW Rst	Retain	
0	Jabber	Mode	RO, LH	0 = No jabber 1 = Jabber
		HW Rst	0	
		SW Rst	Retain	

5.10.19 Smart speed register

Address offset: 0x14, or 0d20

Table 5-388 summarizes the smart speed register.

Table 5-388 Smart speed register bit description

Bits	Symbol	Type		Description
15:11	RESERVED	Mode	RO	Reserved. Must be 00000000.
		HW Rst	0	
		SW Rst	0	
10	ANEG_NOW_QUAL	Mode	R/W	A rise of input pin ANEG_NOW sets this bit to 2, and cause PHY to restart auto-negotiation. Self-cleared.
		HW Rst	0	
		SW Rst	Retain	
9	REV_ANEG_QUAL	Mode	R/W	Make PHY to auto-negotiate in reversed mode. This bit takes its value from the input pin REV_ANEG upon following: 1. HW reset (fall of RST_DSP_I); 2. PHY SW reset; 3. Rise of ANEG_NOW.
		HW Rst	0	
		SW Rst	Update	
8	GIGA_DIS_QUAL	Mode	R/W	Make PHY to disable Gigabit mode. This bit takes its value from the input pin GIGA_DIS upon following: 1. HW reset (fall of RST_DSP_I); 2. PHY SW reset; 3. Rise of ANEG_NOW.
		HW Rst	0	
		SW Rst	Update	

Table 5-388 Smart speed register bit description (cont.)

Bits	Symbol	Type		Description
7	CFG_PAD_EN	Mode	RO, LH	The default value is zero; if this bit is set to one, then the auto-negotiation arbitration FSM bypasses the LINK_STATUS_CHECK state when the 10 base/100 base ready signal is asserted.
		HW Rst	0	
		SW Rst	Retain	
6	MR_LTDIS	Mode	R/W	The default value is zero; if this bit is set to one, then the NLP receive link integrity test FSM stays at the NLP_TEST_PASS state.
		HW Rst	0	
		SW Rst	Update	
5	SMARTSPEED_EN	Mode	R/W	The default value is one; if this bit is set to one and cable inhibits completion of the training phase, then after a few failed attempts, the DSP PHY automatically downgrades the highest ability to the next lower speed; from 1000 to 100 to 10.
		HW Rst	1	
		SW Rst	Update	
4:2	SMARTSPEED_RETRY_LIMIT	Mode	R/W	The default value is three. If these bits are set to three, then the DSP PHY attempts five times before downgrading. The number of attempts can be changed through setting these bits.
		HW Rst	011	
		SW Rst	Update	
1	BYPASS_SMARTSPEED_TIMER	Mode	R/W	The default value is zero. If this bit is set to one, the Smartspeed FSM bypasses the timer used for stability.
		HW Rst	0	
		SW Rst	Update	
0	RESERVED	Mode	RO	Reserved. Must be set to 0.
		HW Rst	0	
		SW Rst	0	

5.10.20 Receive error counter register

Address offset: 0x15, or 0d21

[Table 5-389](#) summarizes the status register.

Table 5-389 Status register bit description

Bits	Symbol	Type		Description
15:0	Receive Error Count	Mode	RO	Counter pegs at 0xFFFF and does not roll over. (When RX_DV is valid, count RX_ER numbers) (In this version, only for 100BASE-Tx and 1000BASE-T)
		HW Rst	0x0000	
		SW Rst	Retain	

5.10.21 Virtual cable tester control register

Address offset: 0x16, or 0d22

[Table 5-390](#) summarizes the virtual cable tester control register.

Table 5-390 Virtual cable tester control register bit description

Bits	Symbol	Type		Description
15:10	RESERVED	Mode	RO	
		HW Rst	Always 0	
		SW Rst	Always 0	
9:8	MDI Pair Select	Mode	R/W	Use the virtual cable tester control registers to select which MDI pair is shown in the virtual cable tester status register. 00 = MDI[0] pair 01 = MDI[1] pair 10 = MDI[2] pair 11 = MDI[3] pair
		HW Rst	00	
		SW Rst	Retain	
7:1	Reserved	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
0	Enable Test	Mode	R/W	When set, hardware automatically disable this bit when VCT is done. 1 = Enable VCT test 0 = Disable VCT test
		HW Rst	0	
		SW Rst	Retain	

5.10.22 Virtual cable tester status register

Address offset: 0x1C, or 0d28

Table 5-391 summarizes the virtual cable tester status register.

Table 5-391 Virtual cable tester status register bit description

Bits	Symbol	Type		Description
15:10	RESERVED	Mode	RO	
		HW Rst	Always 0	
		SW Rst	Always 0	
9:8	STATUS	Mode	RO	Content of the virtual cable tester status registers applies to the cable pair selected in the virtual cable tester control registers. 11 = Linkup state. No open or short in cable. 00 = Valid test. Normal cable (no short or open in cable) 10 = Valid test. Open in cable for MDI pair 0/2; short in cable for MDI pair 1/3 01 = Valid test. Short in cable for MDI pair 0/2; open in cable for MDI pair 1/3
		HW Rst	00	
		SW Rst	00	

Table 5-391 Virtual cable tester status register bit description (cont.)

Bits	Symbol	Type		Description
7:0	DELTA_TIME	Mode	R/W	Delta time to indicate distance. Length = DELTA_TIME * 0.824
		HW Rst	0	
		SW Rst	0	

5.10.23 Debug port

Address offset: 0x1D, or 0d29

Table 5-392 summarizes the debug port (address offset 0x1d, or 0d29).

Table 5-392 Debug port (address offset 0x1d, or 0d29) bit description

Bits	Symbol	Type		Description
15:6	RESERVED	Mode	RO	
		HW Rst	0	
		SW Rst	0	
5:0	Address Offset	Mode	R/W	The address index of the register is written or read.
		HW Rst	0	
		SW Rst	0	

5.10.24 Debug port 2 (R/W port)

Address offset: 0x1E, or 0d30

Table 5-393 summarizes the debug port 2 — R/W port.

Table 5-393 Debug port 2 (R/W port) bit description

Bits	Symbol	Type		Description
15:0	Debug Data Port	Mode	R/W	The data port of debug register. Before access this register, must set the address offset first.
		HW Rst	0	
		SW Rst	0	

5.11 Debug register

5.11.1 Analog test control

Address offset: 0x00, or 0d00

Table 5-394 summarizes the debug register — analog test control.

Table 5-394 Analog test control bit description

Bits	Symbol	Type		Description
15	SEL_CLK125M_DSP	Mode	R/W	Control bit for RGMII interface Rx clock delay: 0 = RGMII Rx clock delay disable 1 = RGMII Rx clock delay enable
		HW Rst	1	
		SW Rst	0	
14:12	RESERVED	Mode	R/W	
		HW Rst	0	
		SW Rst	Retain	
11	RESERVED	Mode	R/W	
		HW Rst	0	
		SW Rst	0	
10	RESERVED	Mode	R/W	
		HW Rst	0	
		SW Rst	Retain	
9	RESERVED	Mode	R/W	
		HW Rst	1	
		SW Rst	Retain	
8	RESERVED	Mode	R/W	
		HW Rst	0	
		SW Rst	Retain	
7:5	RESERVED	Mode	R/W	
		HW Rst	1	
		SW Rst	Retain	
4:3	RESERVED	Mode	R/W	
		HW Rst	2'h1	
		SW Rst	Retain	
2	MANU_SWITCH_ON	Mode	R/W	DAC amplitude adjustment 0 = No increase 1 = Add +6%
		HW Rst	1	
		SW Rst	Retain	
1	RESERVED	Mode	R/W	
		HW Rst	1	
		SW Rst	Retain	
0	RESERVED	Mode	R/W	
		HW Rst	0	
		SW Rst	Retain	

5.11.2 System mode control

Address offset: 0x03

Table 5-395 summarizes the debug register — system mode control.

Table 5-395 System mode control bit description

Bits	Symbol	Type		Description
15	RESERVED	Mode	R/W	
		HW Rst	0	
		SW Rst	0	
14	RESERVED	Mode	R/W	
		HW Rst	0	
		SW Rst	Retain	
13:9	RESERVED	Mode	R/W	
		HW Rst	1	
		SW Rst	0	
8	OUT_MDIO_SW	Mode	R/W	Control the MDIO signal when POWER_DOWN mode is high. 0 = MDIO is valid, driven by inner state 1 = MDIO is 1
		HW Rst	1	
		SW Rst	Retain	
7:4	RESERVED	Mode	R/W	
		HW Rst	4'b1111	
		SW Rst	Retain	
3:0	RESERVED	Mode	R/W	
		HW Rst	4'b1111	
		SW Rst	Retain	
7:5	RESERVED	Mode	R/W	
		HW Rst	1	
		SW Rst	Retain	
4:3	RESERVED	Mode	R/W	
		HW Rst	2'h1	
		SW Rst	Retain	
2	MANU_SWITCH_ON	Mode	R/W	DAC amplitude adjustment 0 = No increase 1 = Add +6%
		HW Rst	1	
		SW Rst	Retain	
1	RESERVED	Mode	R/W	
		HW Rst	1	
		SW Rst	Retain	

Table 5-395 System mode control bit description (cont.)

Bits	Symbol	Type		Description
0	RESERVED	Mode	R/W	
		HW Rst	0	
		SW Rst	Retain	

5.11.3 System control mode

Address offset: 0x05, or 0d05

Table 5-396 summarizes the debug register — system control mode.

Table 5-396 System control mode bit description

Bits	Symbol	Type		Description
15	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
14	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
13	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
12	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
11	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
10	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
9	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
8	GTXCLK_ DELAY	Mode	R/W	RGMII Tx clock delay control bit: 0 = RGMII Tx clock delay disable 1 = RGMII Tx clock delay enable
		HW Rst	0	
		SW Rst	Retain	

Table 5-396 System control mode bit description (cont.)

Bits	Symbol	Type		Description
7	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
6	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
5:4	RES	Mode	R/W	Reserved
		HW Rst	00	
		SW Rst	Retain	
3	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
2	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
1	100_ClassA	Mode	R/W	This bit is 100BASE-Tx Class A and Class AB mode select bit. 0 = 100BASE-Tx Class AB 1 = 100BASE-Tx Class A
		HW Rst	1	
		SW Rst	Retain	
0	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	

5.11.4 HIB control and auto-negotiation test register

Address offset: 0x0B

Table 5-397 summarizes the HIB control and auto-negotiation test register.

Table 5-397 HIB control and auto-negotiation test register bit description

Bits	Symbol	Type		Description
15	PS_HIB_EN	Mode	R/W	Power hibernation control bit 0 = Hibernation disable 1 = Hibernation enable
		HW Rst	1	
		SW Rst	Retain	
14	WAKE_MODE	Mode	R/W	0 = PHY wakes up only by energy detect 1 = PHY wakes up by energy detect or wake-up pin
		HW Rst	0	
		SW Rst	Retain	

Table 5-397 HIB control and auto-negotiation test register bit description (cont.)

Bits	Symbol	Type		Description
13	EN_ANY_CHANGE	Mode	R/W	0 = Turn on/off analog end step by step 1 = Turn on/off analog end at the same time
		HW Rst	1	
		SW Rst	Retain	
12	HIB_PULSE_SW	Mode	R/W	0 = PHY does not send NLP pulse but detects signal from cables at hibernation state 1 = PHY sends NLP pulse and detects signal from cables at hibernation state
		HW Rst	1	
		SW Rst	Retain	
11	GATE_25M_EN_SW	Mode	R/W	Always 1. 0 = The 25 MHz clock of auto-negotiation is not controlled by hibernation 1 = Shut down the 25 MHz clock of auto-negotiation at hibernation state
		HW Rst	1	
		SW Rst	1	
10	SEL_RST_80U	Mode	R/W	Duration of the reset triggered by speed mode change 0 = 240 μ s 1 = 80/120/160/240 μ s (see bits[9:8] of this register)
		HW Rst	1	
		SW Rst	Retain	
9:8	SEL_RST_TIMER	Mode	R/W	Duration configuration for reset timer 00 = 80 μ s 01 = 120 μ s 10 = 160 μ s 11 = 240 μ s
		HW Rst	00	
		SW Rst	Retain	
7	RESERVED	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
6:5	GTX_DLY_VAL	Mode	R/W	GTX clock delay select
		HW Rst	10	
		SW Rst	Retain	
4	BYPASS_BREAK_LINK_TIMER	Mode	R/W	0 = Auto-negotiation state stays at TRANSMIT_DISABLE for about 1.2 second when auto-negotiation is restarted 1 = BREAL_LINK timer is bypassed when auto-negotiation is restarted, thus auto-negotiation state stays at TRANSMIT_DISABLE for one cycle (40 ns)
		HW Rst	0	
		SW Rst	Retain	
3	DBG_LINK_OK_100T	Mode	R/W	For link management use. The forced LINK_OK_100BT
		HW Rst	0	
		SW Rst	0	
2	DBG_LINK_OK_1000T	Mode	R/W	For link management use. The forced LINK_OK_1000BT
		HW Rst	0	
		SW Rst	0	

Table 5-397 HIB control and auto-negotiation test register bit description (cont.)

Bits	Symbol	Type		Description
1	DBG_LINK_RDY_100T	Mode	R/W	For link management use. The forced LINK_RDY_100BT
		HW Rst	0	
		SW Rst	0	
0	DBG_EN_EN	Mode	R/W	For link management use. When this bit is set, the test bits in this register take effect.
		HW Rst	0	
		SW Rst	0	

5.11.5 RGMII mode selection

Address offset: 0x012, or 0d18

Table 5-398 summarizes the debug register — RGMII mode selection.

Table 5-398 RGMII mode selection bit description

Bits	Symbol	Type		Description
15:14	RES	Mode	R/W	Reserved
		HW Rst	01	
		SW Rst	Retain	
13:12	RES	Mode	R/W	Reserved
		HW Rst	00	
		SW Rst	Retain	
11	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
10	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
9:6	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
5	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	
4	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	

Table 5-398 RGMII mode selection bit description (cont.)

Bits	Symbol	Type		Description
3	RGMII_MODE	Mode	R/W	0 = Select GMII/MII interface with MAC 1 = Select RGMII interface with MAC
		HW Rst	0	
		SW Rst	Retain	
2	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	1	
1:0	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	

5.11.6 Green feature configure register

Address offset: 0x3D

Table 5-399 summarizes the debug register — green feature configure register.

Table 5-399 Green feature configure register bit description

Bits	Symbol	Type		Description
15	RESERVED	Mode	R/W	
		HW Rst	0	
		SW Rst	Retain	
14	RESERVED			
13:8	RESERVED	Mode	R/W	
		HW Rst	6'h28	
		SW Rst	Retain	
7	RESERVED	Mode	R/W	
		HW Rst	1	
		SW Rst	Retain	
6	GATE_CLK_IN1000	Mode	R/W	0 = When in 1000BASE-T mode, gate dig100/dig10/vct clk 1 = When in 1000BASE-T mode, do not gate dig100/dig10/vct clk
		HW Rst	1	
		SW Rst	Retain	
5:0	RESERVED	Mode	R/W	
		HW Rst	6'h20	
		SW Rst	Retain	

5.12 MMD3 — PCS register

5.12.1 PCS control1

Device address: 3, Address offset: 0x00, or 0d00

Table 5-400 summarizes the PCS control 1 register.

Table 5-400 PCS control1 bit description

Bits	Symbol	Type		Description
15	PCS_RST	Mode	R/W	Reset bit, self-cleared. When write this bit 1: 1. Reset the registers (not vender specific) in MMD3/MMD7. 2. Cause software reset in MII register0 bit[15].
		HW Rst	0	
		SW Rst	0	
14:11	RESERVED	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
10	CLOCK_STOPPABLE	Mode	R/W	Not implemented
		HW Rst	1	
		SW Rst	Retain	
9:0	RESERVED	Mode	R/W	Always 0.
		HW Rst	1	
		SW Rst	Retain	

5.12.2 PCS status1

Device address: 3, Address offset: 0x01, or 0d01

Table 5-401 summarizes the PCS status 1 register.

Table 5-401 PCS status1 bit description

Bits	Symbol	Type		Description
15:12	Reserved	Mode	R/W	Always 0.
		HW Rst	0	
		SW Rst	0	
11	Tx LP idle received	Mode	RO	When read as 1, it indicates that the transmit PCS has received low power idle signaling one or more times since the register was last read. Latch high.
		HW Rst	0	
		SW Rst	0	

Table 5-401 PCS status1 bit description (cont.)

Bits	Symbol	Type		Description
10	Rx LP idle received	Mode	R/W	When read as 1, it indicates that the receive PCS has received low power idle signaling one or more times since the register was last read. Latch high.
		HW Rst	0	
		SW Rst	0	
9	Tx LP idle indication	Mode	R/W	When read as 1, it indicates that the transmit PCS is currently receiving low power idle signals.
		HW Rst	0	
		SW Rst	0	
8	Rx LP idle indication	Mode	R/W	When read as 1, it indicates that the receive PCS is currently receiving low power idle signals.
		HW Rst	0	
		SW Rst	0	
7:0	Reserved	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	

5.12.3 EEE capability register

Device address: 3, Address offset: 0x014, or 0d020

Table 5-402 summarizes the EEE capacity register.

Table 5-402 EEE capability register bit description

Bits	Symbol	Type		Description
15:3	RESERVED	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
2	1000BT EEE	Mode	RO	EEE is supported for 1000BASE-T.
		HW Rst	1	
		SW Rst	1	
1	100BT EEE	Mode	RO	EEE is supported for 100BASE-Tx.
		HW Rst	1	
		SW Rst	1	
0	RESERVED	Mode	R/W	Always 0.
		HW Rst	0	
		SW Rst	0	

5.12.4 EEE wake error counter

Device address: 3, Address offset: 0x016, or 0d022

Table 5-403 summarizes the EEE wake error register.

Table 5-403 EEE wake error counter bit description

Bits	Symbol	Type		Description
		Mode	RO	
15:0	EEE Wake Error Counter	Mode	RO	Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.
		HW Rst	0	
		SW Rst	0	This counter is clear after read, and hold at all ones in the case of overflow.

5.13 MMD7 — auto-negotiation register

Device address: 7, Address offset: 0x0, or 0d0

Table 5-404 summarizes the MMD7 — auto-negotiation register.

Table 5-404 AN control 1 bit description

Bits	Symbol	Type		Description
		Mode	RO	
15	AN_RST	Mode	RO	Reset bit, self-clear.
		HW Rst	0	When write this bit 1: 1. Reset the registers (not vender-specific) in MMD3/MMD7. 2. Cause software reset in MII register0 bit[15].
		SW Rst	0	
14	RESERVED	Mode	RO	Always 0.
		HW Rst	1	
		SW Rst	1	
13	XNP_CTRL	Mode	RO	If MII register 4 bit[12] is set to 0, setting of this bit shall have no effect. 0 = Local device does not intend to enable the exchange of extended next page. 1 = Local device intends to enable the exchange of extended next page.
		HW Rst	1	
		SW Rst	1	
12:0	RESERVED	Mode	R/W	Always 0.
		HW Rst	0	
		SW Rst	0	

5.13.1 AN package

Device address: 7, Address offset: 0x05, or 0d05

Table 5-405 summarizes the AN package.

Table 5-405 AN package bit description

Bits	Symbol	Type		Description
		Mode	RO	
15:8	RESERVED	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
7	AUTO_NEG_PRESENT	Mode	RO	Always 1.
		HW Rst	1	
		SW Rst	1	
6:4	RESERVED	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
3	PCS PRESENT	Mode	RO	Always 1.
		HW Rst	1	
		SW Rst	1	
2:1	RESERVED	Mode	R/W	Always 0.
		HW Rst	0	
		SW Rst	0	
0	MII_REG_PRESENT	Mode	R/W	Always 1.
		HW Rst	1	
		SW Rst	1	

5.13.2 AN status

Device address: 7, Address offset: 0x01, or 0d1

Table 5-406 summarizes the AN status.

Table 5-406 AN status bit description

Bits	Symbol	Type		Description
		Mode	RO	
15:8	RESERVED	Mode	RO	
		HW Rst	0	
		SW Rst	0	
7	XNP_STATUS	Mode	RO	0 = Extended next page shall not be used. 1 = Both local device and link partner have indicated support for extended next page.
		HW Rst	0	
		SW Rst	0	
6:0	RESERVED	Mode	RO	
		HW Rst	0	
		SW Rst	0	

5.13.3 AN XNP transmit

Device address: 7, Address offset: 0x016, or 0d22

Table 5-407 summarizes the AN XNP transmit register.

Table 5-407 AN XNP transmit bit description

Bits	Symbol	Type		Description
15:0	XNP_22	Mode	RO	A write to this register set MR_NEXT_PAGE_LOADED.
		HW Rst	0	
		SW Rst	0	

5.13.4 AN XNP transmit1

Device address: 7, Address offset: 0x017, or 0d23

Table 5-408 summarizes the AN XNP transmit 1 register.

Table 5-408 AN XNP transmit1 bit description

Bits	Symbol	Type		Description
15:0	XNP_23	Mode	RO	
		HW Rst	0	
		SW Rst	0	

5.13.5 AN XNP transmit 2

Device address: 7, Address offset: 0x018, or 0d24

Table 5-409 summarizes the AN XNP transmit 2 register.

Table 5-409 AN XNP transmit2 bit description

Bits	Symbol	Type		Description
15:0	XNP_23	Mode	RO	
		HW Rst	0	
		SW Rst	0	

5.13.6 AN LP XNP ability

Device address: 7, Address offset: 0x019, or 0d25

Table 5-410 summarizes the AN LP XNP ability register.

Table 5-410 AN LP XNP ability bit description

Bits	Symbol	Type		Description
15:0	XNP_23	Mode	RO	
		HW Rst	15'h0	
		SW Rst	15'h0	

5.13.7 AN LP XNP ability1

Device address: 7, Address offset: 0x01A, or 0d26

Table 5-411 summarizes the AN LP XNP ability 1 register.

Table 5-411 AN LP XNP ability1 bit description

Bits	Symbol	Type		Description
15:0	LP_XNP_2	Mode	RO	Latched when LP_XNP_1 is read
		HW Rst	15'h0	
		SW Rst	15'h0	

5.13.8 AN LP XNP ability2

Device address: 7, Address offset: 0x01B, or 0d27

Table 5-412 summarizes the AN LP XNP ability2 register.

Table 5-412 AN LP XNP ability2 bit description

Bits	Symbol	Type		Description
15:0	LP_XNP_3	Mode	RO	Latched when LP_XNP_1 is read
		HW Rst	15'h0	
		SW Rst	15'h0	

5.13.9 EEE advertisement

Device address: 7, Address offset: 0x3C (Hex)

Table 5-413 summarizes the EEE advertisement register.

Table 5-413 EEE advertisement bit description

Bits	Symbol	Type		Description
15:3	RESERVED	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
2	EEE_1000BT	Mode	R/W	If local device supports EEE operation for 1000BASE-T, and EEE operation is desired, this bit shall be set to 1.
		HW Rst	1	
		SW Rst	Retain	
1	EEE_100BT	Mode	R/W	If local device supports EEE operation for 100BASE-Tx, and EEE operation is desired, this bit shall be set to 1.
		HW Rst	1	
		SW Rst	Retain	
0	RESERVED	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	

5.13.10 EEE LP advertisement

Device address: 7, Address offset: 0x3D (Hex)

Table 5-414 summarizes the EEE LP advertisement register.

Table 5-414 EEE LP advertisement bit description

Bits	Symbol	Type		Description
15:3	RESERVED	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
2	EEE_1000BT	Mode	RO	If local device supports EEE operation for 1000BASE-T, and EEE operation is desired, this bit shall be set to 1.
		HW Rst	0	
		SW Rst	0	
1	EEE_100BT	Mode	RO	If local device supports EEE operation for 100BASE-Tx, and EEE operation is desired, this bit shall be set to 1.
		HW Rst	0	
		SW Rst	0	
0	RESERVED	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	

5.13.11 EEE ability auto-negotiation result

Device address: 7, Address offset: 0x8000 (Hex)

Table 5-415 summarizes the EEE ability auto-negotiation result register.

Table 5-415 EEE ability auto-negotiation result bit description

Bits	Symbol	Type		Description
15:3	RESERVED	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
2	EEE_1000BT_EN	Mode	RO	0 = 1000BASE-T az disable; either side does not support EEE operation for 1000BT, or EEE operation is not desired. 1 = 1000BASE-T az enable; both sides support EEE operation for 1000BT, and EEE operation is desired.
		HW Rst	0	
		SW Rst	0	
1	EEE_100BT_EN	Mode	RO	0 = 100BASE-Tx az disable; either side does not support EEE operation for 100BASE-Tx, or EEE operation is not desired. 1 = 100BASE-Tx az enable; both sides support EEE operation for 100BASE-Tx, and EEE operation is desired.
		HW Rst	0	
		SW Rst	0	
0	RESERVED	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	

6 Package Dimensions

The QCA8337N is packaged in a 148-pin DR-QFN. The body size is 12 mm by 12 mm. The package drawings and dimensions are provided in [Figure 6-1](#) and [Table 6-1](#).

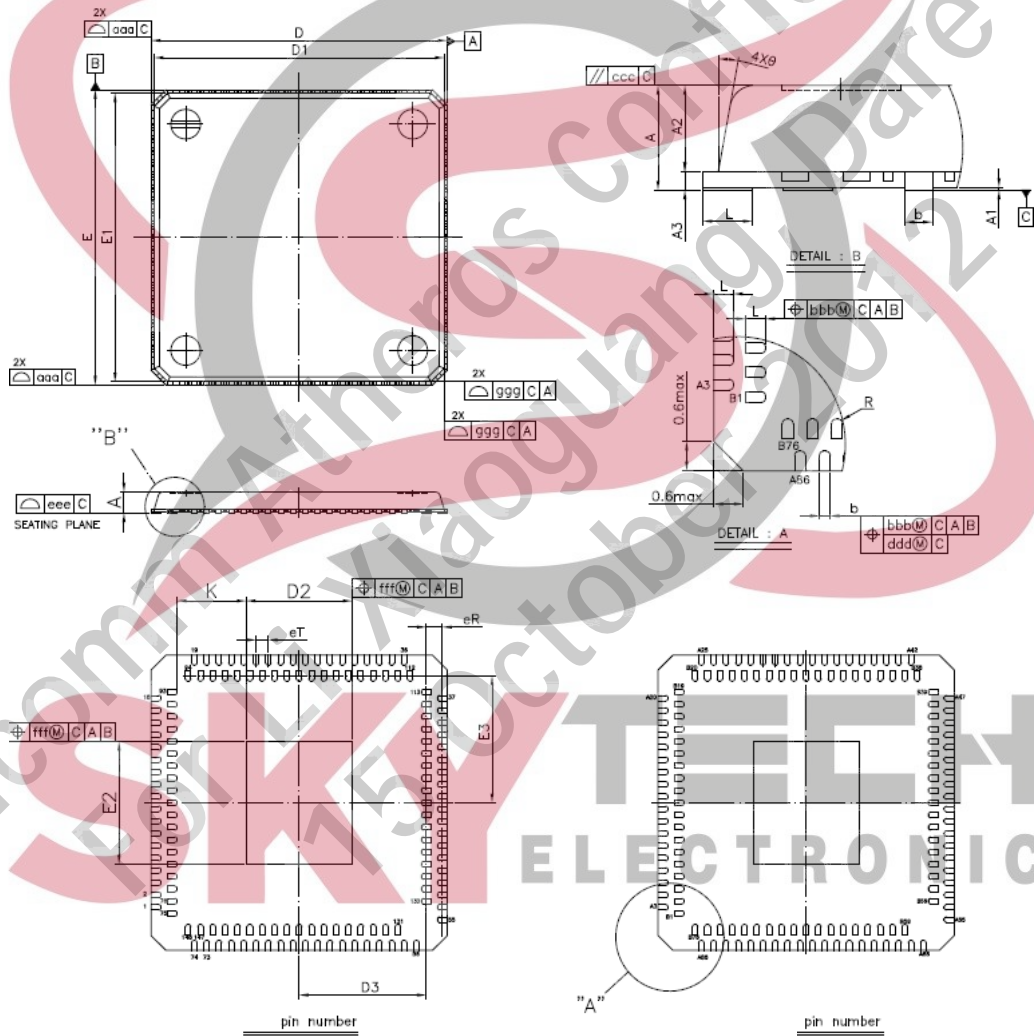


Figure 6-1 148-pin DR-QFN package drawing

Table 6-1 Package dimensions (in mm)

Symbol	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm
A1	0.00	0.02	0.05	mm
A2	0.65	0.70	0.75	mm
A3	0.15 REF			mm
b	0.18	0.22	0.30	mm
D/E	11.90	12.00	12.10	mm
D1/E1	11.75 BSC			mm
D2	5.40	5.50	5.60	mm
E2	6.40	6.50	6.60	mm
D3/E3	5.15 BSC			mm
eT	0.50 BSC			mm
eR	0.65 BSC			mm
L	0.30	0.40	0.50	mm
θ	5	—	15	°
K	0.20	—	—	mm
R	0.09	—	—	mm
aaa	0.10			mm
bbb	0.10			mm
ccc	0.10			mm
ddd	0.05			mm
eee	0.08			mm
fff	0.10			mm
ggg	0.20			mm

7 Ordering Information

The order information is listed in [Table 7-1](#).

Table 7-1 Ordering information

Ordering number	Package	Ambient temperature	Default ordering unit
QCA8337N-AL3C	DR-QFN 148-pin (12 nm x 12 nm)	Commercial (0–70 °C)	Tray
QCA8337N-AL3B	DR-QFN 148-pin (12 nm x 12 nm)	Industrial (-40–85°C)	Tray



8 Top-Side Marking

The top-side marking is listed in [Figure 8-1](#).

Table 8-1 Top-side marking

Ordering number	Marking
QCA8337N-AL3C	QCA8337N-AL3C
QCA8337N-AL3B	QCA8337N-AL3B

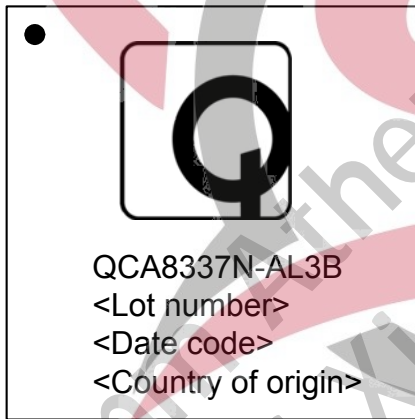


Figure 8-1 Top-side marking

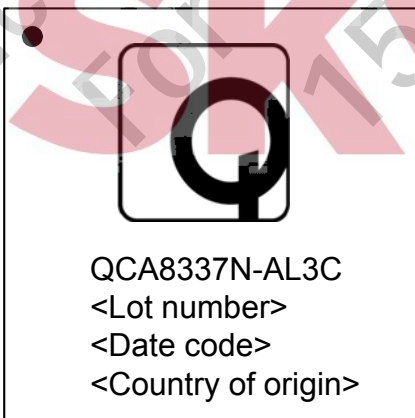


Figure 8-2 Top-side marking

